QDD4-400GB-DR4-AO

MSA and TAA 400GBase-DR4 QSFP-DD Transceiver (SMF, 1310nm, 500m, MPO, DOM, CMIS 4.0)

Features

- QSFP-DD MSA compliant
- IEEE 802.3bs 400GBASE-DR4 Specification compliant
- Parallel 4 Optical Lanes
- Data Rate 106.25Gbps (PAM4) per channel
- Commercial Temperature 0 to 70 Celsius
- 8x53.125Gb/s electrical interface (400GAUI-8)
- MPO-12 connector
- Maximum power consumption 10.5W
- RoHS compliant and Lead Free

Applications

- 400GBase Etherent

Product Description

This MSA Compliant QSFP-DD transceiver provides 400GBase-DR4 throughput up to 500m over single-mode fiber (SMF) using a wavelength of 1310nm via an MPO connector. It is built to MSA standards and is uniquely serialized and data-traffic and application tested to ensure that they will integrate into your network seamlessly. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."

TAA COMPLIANT

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	-0.5		3.6	V	
Storage Temperature	Tstg	-40		85	°C	
Case Operating Temperature	Tc	0		70	°C	
Relative Humidity	RH	0		85	%	Non-Condensing
Damage Threshold Per Lane	THd	5			dBm	
Data Rate Per Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance	D	2		500	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Current	Icc			3.18	A	
Power Consumption	PD			10.5	W	
Transmitter						
Signaling Rate Per Lane	TP1	26.5625 ± 100ppm			GBd	
Differential Pk-Pk Input Voltage Tolerance	TP1a	900			mVp-p	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common-Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1				2
Single-Ended Voltage Tolerance Range (Minimum)	TP1a	-0.4 to 3.3			V	
DC Common-Mode Input Voltage	TP1	-350		2850	mV	3
Receiver						
Signaling Rate Per Lane	TP4	26.5625 ± 100ppm			GBd	
Differential Pk-Pk Output Voltage	TP4			900	mVp-p	
AC Common-Mode Output Voltage (RMS)	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3-2015 Equation (83E-2)				
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3-2015 Equation (83E-3)				
Transition Time (20-80%)	TP4	9.5			ps	
Near-End Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-End Eye Height (Differential)	TP4	70			mV	
Far-End Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-End Eye Height (Differential)	TP4	30			mV	
Far-End Pre-Cursor ISI Ratio	TP4	-4.5		2.5	%	
Common-Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E.1.1.
3. DC common-mode voltage generated by the host. Specification includes effects of ground offset voltage.

Optical Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter							
Data Rate Per Lane			53.125 ± 100ppm			GBd	
Modulation Format			PAM4				
Center Wavelength		λC	1304.5	1310	1317.5	nm	
Side-Mode Suppression Ratio		SMSR	30			dB	
Average Launch Power Per Lane		Pavg	-2.9		4	dBm	1
Outer Optical Modulation Amplitude (OMA_{outer}) Per Lane		POMA	-0.8		4.2	dBm	2
Launch Power in OMA_{outer} Minus TDECQ Per Lane	**For ER≥5dB**		-2.2			dB	
	For ER≤5dB		-1.9			dB	
Transmitter and Dispersion Eye Closure for PAM4 Per Lane		TDECQ			3.4	dB	
TDECQ – $10*log_{10}$ (C_{eq}) Per Lane					3.4	dB	3
Extinction Ratio		ER	3.5			dB	
$RIN_{21.4}OMA$		RIN			-136	dB/Hz	
Optical Return Loss Tolerance		TOL			21.4	dB	
Transmitter Reflectance		T_R			-26	dB	
Transmitter Transition Time					17	ps	
Average Launch Power of Off Transmitter Per Lane		Poff			-15	dBm	
Receiver							
Center Wavelength		λC	1304.5	1310	1317.5	nm	
Data Rate Per Lane			53.125 ± 100ppm			GBd	
Modulation Format			PAM4				
Damage Threshold Per Lane		TH_d	5			dBm	4
Average Receive Power Per Lane			-5.9		4	dBm	5
Receive Power (OMA_{outer}) Per Lane					4.2	dBm	
Receiver Sensitivity (OMA_{outer}) Per Lane		SEN			Equation (1)	dBm	6
Stressed Receiver Sensitivity (OMA_{outer}) Per Lane		SRS			-1.9	dBm	7
Receiver Reflectance		R_R			-26	dB	
LOS Assert		LOSA	-15			dBm	
LOS De-Assert		LOSD			-8.9	dBm	
LOS Hysteresis		LOSH	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 8)							
Stressed Eye Closure for PAM4 (SECQ) Lane Under Test				3.4		dB	

SECQ – 10*log$_{10}$ (Ceq) Per Lane Under Test				3.4	dB	
OMA$_{outer}$ of Each Aggressor Lane			4.2		dBm	

Notes:

1. Average launch power, each lane (minimum), is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. Even if the TDECQ<1.4dB for an extinction ratio of ≥5dB or TDECQ<1.1dB for an extinction ratio of <5dB, the OMA$_{outer}$ (minimum) must exceed the minimum value specified here.
3. Ceq is a coefficient defined in IEEE Std 802.3-2018 Clause 121.8.5.3 which accounts for reference equalizer noise enhancement.
4. Average receive power, each lane (minimum), is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
6. Receiver sensitivity (OMAouter), each lane (maximum), is informative and is defined for a transmitter with a value of SECQ up to 3.4 dB. It should meet Equation (1), which is illustrated in below:

$$RS = \text{Max.}(-3.9, SECQ - 5.3)\ dBm \quad (1)$$

Where:

RS is the receiver sensitivity, and

SECQ is the SECQ of the transmitter used to measure the receiver sensitivity.

7. Measured with conformance test signal at TP3 for the BER equal to 2.4x10^{-4}.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

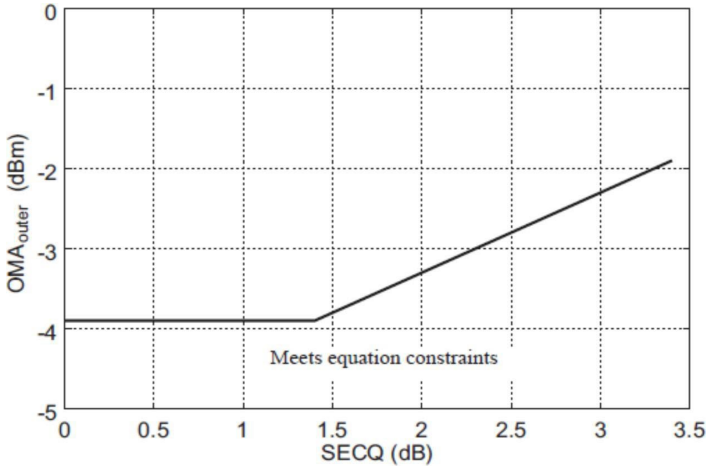


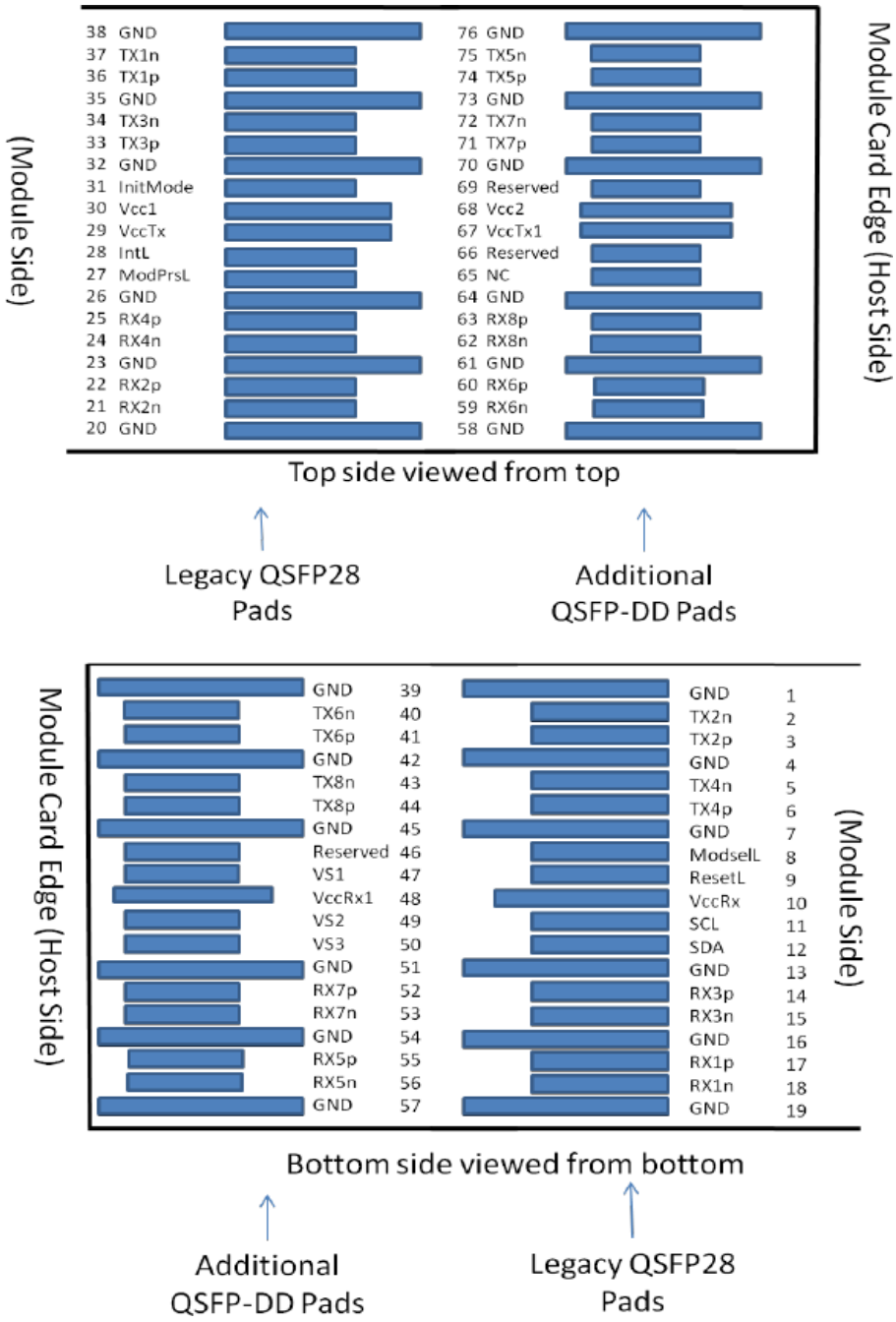
Illustration of Receiver Sensitivity Mask for 400G-DR4

Pin Descriptions

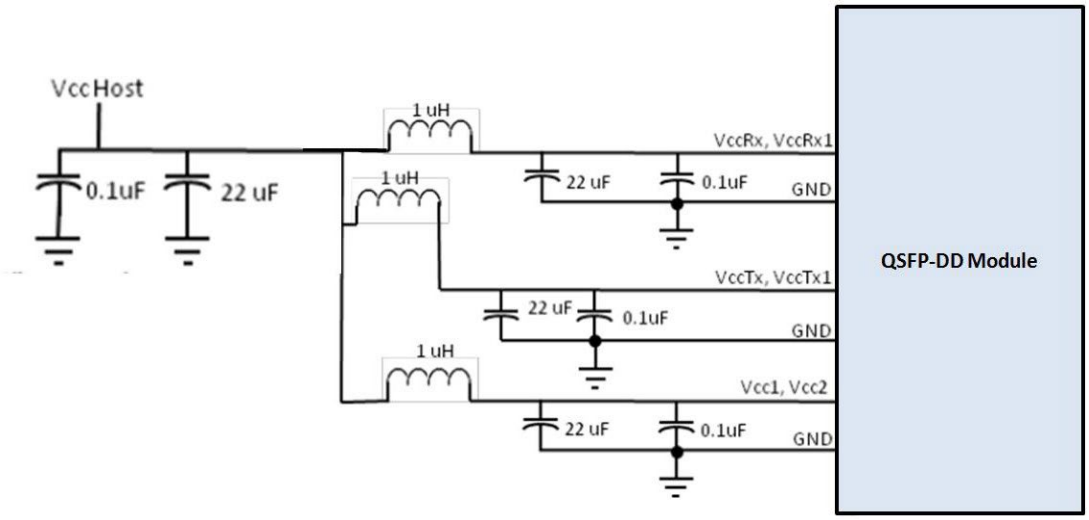
Pin	Logic	Symbol	Name/Description	Plug Sequence
1		GND	Module Ground.	1B
2	CML-I	Tx2-	Transmitter Inverted Data Input.	3B
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	3B
4		GND	Module Ground.	1B
5	CML-I	Tx4-	Transmitter Inverted Data Input.	3B
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	3B
7		GND	Module Ground.	1B
8	LVTTL-I	ModSelL	Module Select.	3B
9	LVTTL-I	ResetL	Module Reset.	3B
10		VccRx	+3.3V Receiver Power Supply.	2B
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	3B
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	3B
13		GND	Module Ground.	1B
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	3B
15	CML-O	Rx3-	Receiver Inverted Data Output.	3B
16		GND	Module Ground.	1B
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	3B
18	CML-O	Rx1-	Receiver Inverted Data Output.	3B
19		GND	Module Ground.	1B
20		GND	Module Ground.	1B
21	CML-O	Rx2-	Receiver Inverted Data Output.	3B
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	3B
23		GND	Module Ground.	1B
24	CML-O	Rx4-	Receiver Inverted Data Output.	3B
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	3B
26		GND	Module Ground.	1B
27	LVTTL-O	ModPrsL	Module Present.	3B
28	LVTTL-O	IntL	Interrupt.	3B
29		VccTx	+3.3V Transmitter Power Supply.	2B
30		Vcc1	+3.3V Power Supply.	2B
31	LVTTL-I	InitMode	Initialization Mode. In legacy QSFP applications, the InitMode pad is called LPMode.	3B
32		GND	Module Ground.	1B
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	3B
34	CML-I	Tx3-	Transmitter Inverted Data Input.	3B
35		GND	Module Ground.	1B
36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	3B
37	CML-I	Tx1-	Transmitter Inverted Data Input.	3B
38		GND	Module Ground.	1B

39		GND	Module Ground.	1A
40	CML-I	Tx6-	Transmitter Inverted Data Input.	3A
41	CML-I	Tx6+	Transmitter Non-Inverted Data Input.	3A
42		GND	Module Ground.	1A
43	CML-I	Tx8-	Transmitter Inverted Data Input.	3A
44	CML-I	Tx8+	Transmitter Non-Inverted Data Input.	3A
45		GND	Module Ground.	1A
46		Reserved	For Future Use.	3A
47		VS1	Module Vendor-Specific 1.	3A
48		VccRx1	+3.3V Receiver Power Supply.	2A
49		VS2	Module Vendor-Specific 2.	3A
50		VS3	Module Vendor-Specific 3.	3A
51		GND	Module Ground.	1A
52	CML-O	Rx7+	Receiver Non-Inverted Data Output.	3A
53	CML-O	Rx7-	Receiver Inverted Data Output.	3A
54		GND	Module Ground.	1A
55	CML-O	Rx5+	Receiver Non-Inverted Data Output.	3A
56	CML-O	Rx5-	Receiver Inverted Data Output.	3A
57		GND	Module Ground.	1A
58		GND	Module Ground.	1A
59	CML-O	Rx6-	Receiver Inverted Data Output.	3A
60	CML-O	Rx6+	Receiver Non-Inverted Data Output.	3A
61		GND	Module Ground.	1A
62	CML-O	Rx8-	Receiver Inverted Data Output.	3A
63	CML-O	Rx8+	Receiver Non-Inverted Data Output.	3A
67		GND	Module Ground.	1A
68		NC	Not Connected.	3A
69		Reserved	For Future Use.	3A
70		VccTx1	+3.3V Transmitter Power Supply.	2A
71		Vcc2	+3.3V Power Supply.	2A
72		Reserved	For Future Use.	3A
73		GND	Module Ground.	1A
74	CML-I	Tx7+	Transmitter Non-Inverted Data Input.	3A
75	CML-I	Tx7-	Transmitter Inverted Data Input.	3A
76		GND	Module Ground.	1A

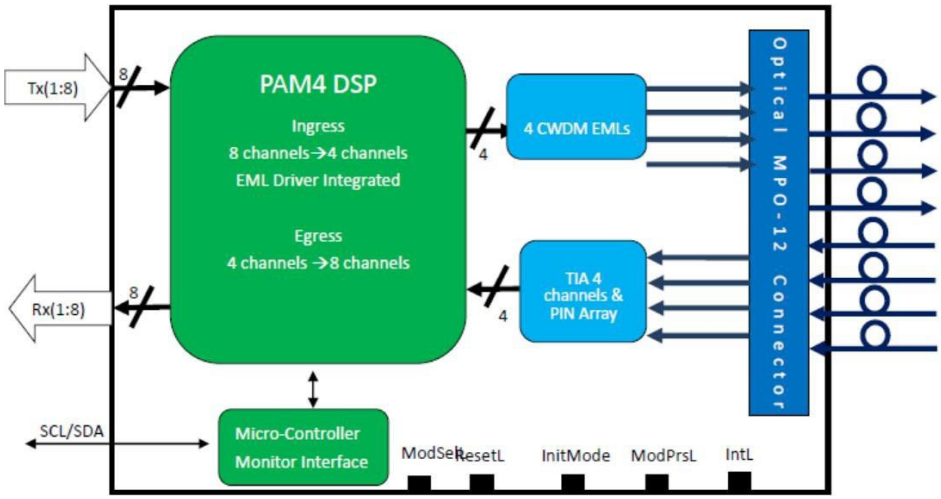
Electrical Pin-Out Details



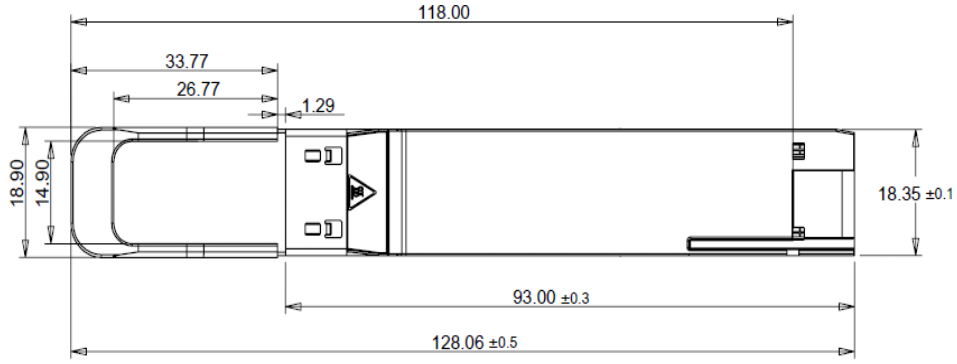
Recommended Power Supply Filter

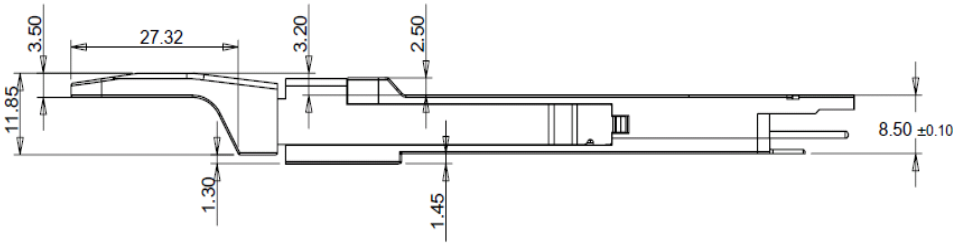


Block Diagram



Mechanical Specifications





About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is in engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.

U.S. Headquarters

Email: sales@addonnetworks.com

Telephone: +1 877.292.1701

Fax: 949.266.9273

Europe Headquarters

Email: salessupportemea@addonnetworks.com

Telephone: +44 1285 842070