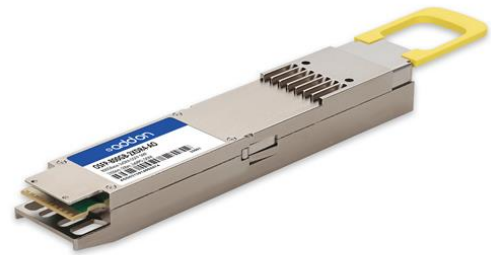


OSFP-800GB-2XDR4-AO

MSA and TAA 800GBase-2xDR4 PAM4 OSFP Transceiver (SMF, 1310nm, 500m, 2xMPO, DOM, CMIS 5.0)

Features

- OSFP MSA Compliant
- Supports 850Gbps
- 8x53.125Gb/s (PAM4) Electrical Interface
- Compliant with IEEE 802.3cu-2021: 8x100GBASE-DR optical interface
- Compliant with IEEE 802.3ck-2022: 8x100GAUI-1 C2M electrical interface
- Support both Ethernet and InfiniBand NDR
- EML transmitter and PIN PD receiver
- Commercial Temperature: 0 to 70 Celsius
- Class 1 Laser
- Dual MPO-12 Connector APC
- RoHS Compliant and Lead-Free



Applications

- 2x400GBase Ethernet
- 8x100GBase Ethernet

Product Description

This MSA Compliant OSFP transceiver provides 800GBase-2xDR4 throughput up to 500m over single-mode fiber (SMF) using a wavelength of 1310nm via a 2xMPO connector. It is built to MSA standards and is uniquely serialized and data-traffic and application tested to ensure that they will integrate into your network seamlessly. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	V _{CC}	-0.5		3.6	V	
Storage Temperature	T _{stg}	-40		85	°C	
Operating Case Temperature	T _c	0		70	°C	
Relative Humidity (non-condensing)	RH	5		95	%	
Data Input Voltage Differential	V _{DIP-V_{DIN}}			1	V	
Control Input Voltage	V _I	-0.3		V _{CC} +0.5	V	
Control Output Current	I _O	-20		20	mA	
Signaling Speed per Lane	DRL		53.125		GBd	
Operating Distance		2		500	m	

Notes:

- Exceeding the Absolute Maximum Ratings table may cause permanent damage to the device. This is just an emphasized rating and does not involve the functional operation of the device that exceeds the specifications of this technical specification under these or other conditions. Long-term operation under Absolute Maximum Ratings will affect the reliability of the device.

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	V _{CC}	3.135	3.3	3.465	V	
Instantaneous peak current at hot plug	I _{CC_IP}			6600	mA	
Sustained peak current at hot plug	I _{CC_SP}			5494.5	mA	
Maximum Power Dissipation	P _D			16.5	W	
Maximum Power Dissipation, Low Power Mode	P _{DLP}			2	W	
Control Input Voltage High	V _{IH}	V _{CC} *0.7		V _{CC} +0.3	V	
Control Input Voltage Low	V _{IL}	-0.3		V _{CC} *0.3	V	
Two Wire Serial Interface Clock Rate				400	kHz	
Power Supply Noise 1 kHz - 1 MHz (p-p)				66	mVpp	
High-Speed Electrical Transmitter Characteristics (TP1)						
Differential Peak-Peak Input Voltage Tolerance		750			mV	
Peak-to-Peak AC Common-Mode Voltage Tolerance	Low-frequency, V _{CM_LF}			32	mV	
	Full-band, V _{CM_FB}			80	mV	
Differential-mode to common-mode return loss	RL _{cd}	802.3ck 120G-2			dB	
Effective return loss	ERL	8.5			dB	
Differential termination mismatch				10	%	

Single-ended voltage tolerance range			-0.4		3.3	V	
DC common-mode voltage tolerance			-0.35		2.85	V	
High-Speed Electrical Receiver Characteristics (TP4)							
Peak-to-Peak AC Common-Mode Voltage	Low-frequency, $V_{CM_{LF}}$				32	mV	
	Full-band, $V_{CM_{FB}}$				80	mV	
Differential Peak-to-Peak Output Voltage	Short Mode				600	mV	
	Long Mode				845	mV	
Eye height	EH	15				mV	
Vertical eye closure	VEC				12	dB	
Common-mode to differential-mode return loss	RLDc	802.3ck 120G-1				dB	
Effective return loss	ERL	8.5				dB	
Differential termination mismatch					10	%	
Transition time		8.5				ps	
DC common-mode voltage tolerance			-0.35		2.85	V	

Notes:

1. Compliant with IEEE802.3ck C2M.

Electrical Low Speed Control and Sense Signals Specifications

Parameter	Symbol	Min.	Max.	Unit	Notes
Module output SCL and SDA	VOL	0	0.4	V	
Module Input SCL and SDA	VIL	-0.3	VCC*0.3	V	
	VIH	VCC*0.7	VCC+0.5	V	
InitMode, ResetL and ModSelL	VIL	-0.3	0.8	V	
	VIH	2	VCC+0.3	V	
IntL	VOL	0	0.4	V	
	VOH	VCC-0.5	VCC+0.3	V	

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Wavelength	λ_C	1304.5	1311	1317.5	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each lane	AOPL	-2.9		4.0	dBm	1
Outer Optical Modulation Amplitude (OMA _{outer}), each Lane	TOMA	-0.8		4.2	dBm	
Launch power in OMA _{outer} Minus TDECQ, each lane	for extinction ratio ≥ 5 dB	TOMA-TDECQ	-2.2		dBm	
	for extinction ratio < 5 dB	TOMA-TDECQ	-1.9		dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ			3.4	dB	
TDECQ – $10\log_{10}(C_{eq})$, each lane	C _{eq}			3.4	dB	
Average Launch Power of OFF Transmitter, each lane	TOFF			-15	dBm	
Extinction Ratio	ER	3.5			dB	
Transmitter Transition Time	T _r			17	ps	
RIN _{15.5,OMA}	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORL			15.5	dB	
Transmitter Reflectance	T _R			-26	dB	2
Receiver						
Wavelength	λ_{C0}	1304.5	1311	1317.5	nm	
Damage Threshold, each Lane	AOP _D	5			dBm	
Average Receive Power, each Lane	AOP _R	-5.9		4	dBm	
Receive Power (OMA _{outer}), each Lane	OMA _R			4.2	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMA _{outer}), each Lane	SOMA			Max (-3.9, SECQ – 5.3)	dBm	3
Stressed Receiver Sensitivity (OMA _{outer}), each Lane	SRS			-1.9	dBm	4
Conditions of Stressed Receiver Sensitivity Test						
Stressed Eye Closure for PAM4 (SECQ), Lane Under Test	SECQ		3.4		dB	
SECQ – $10\log_{10}(C_{eq})$, Lane Under Test	C _{eq}			3.4	dB	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. Transmitter reflectance is defined looking into the transmitter.
3. Receiver sensitivity (OMA_{outer}), each lane (max) is informative and is defined for a transmitter with a value of SECQ up to 3.4dB.
4. Measured with conformance test signal at TP3 for the BER = 2.4×10^{-4} .

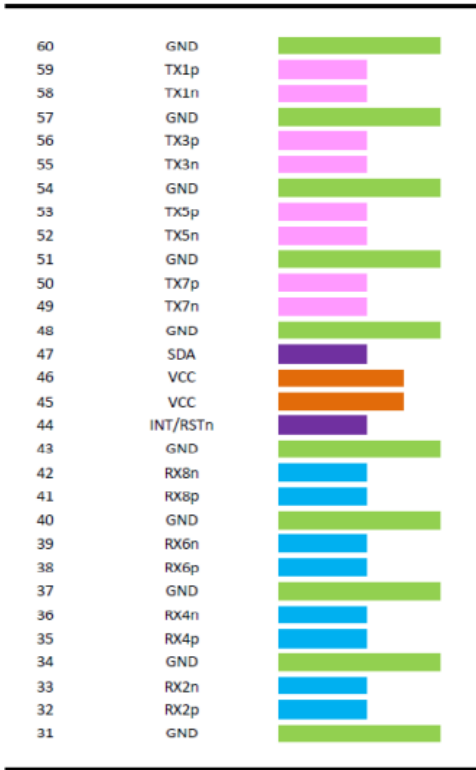
Pin Descriptions

Pin	Logic	Symbol	Name/Description	Notes
1		GND	Module Ground.	
2	CML-I	Tx2+	Transmitter Non-Inverted Data.	
3	CML-I	Tx2-	Transmitter Inverted Data.	
4		GND	Module Ground.	
5	CML-I	Tx4+	Transmitter Non-Inverted Data.	
6	CML-I	Tx4-	Transmitter Inverted Data.	
7		GND	Module Ground.	
8	CML-I	Tx6+	Transmitter Non-Inverted Data.	
9	CML-I	Tx6-	Transmitter Inverted Data.	
10		GND	Module Ground.	
11	CML-I	Tx8+	Transmitter Non-Inverted Data.	
12	CML-I	Tx8-	Transmitter Inverted Data.	
13		GND	Module Ground.	
14	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock.	
15		Vcc	+3.3V Power Supply.	
16		Vcc	+3.3V Power Supply.	
17	Multi-Level	LPWn/PRSn	Low-Power Mode/Module Present.	
18		GND	Module Ground.	
19	CML-O	Rx7-	Receiver Inverted Data.	
20	CML-O	Rx7+	Receiver Non-Inverted Data.	
21		GND	Module Ground.	
22	CML-O	Rx5-	Receiver Inverted Data.	
23	CML-O	Rx5+	Receiver Non-Inverted Data.	
24		GND	Module Ground.	
25	CML-O	Rx3-	Receiver Inverted Data.	
26	CML-O	Rx3+	Receiver Non-Inverted Data.	
27		GND	Module Ground.	
28	CML-O	Rx1-	Receiver Inverted Data.	
29	CML-O	Rx1+	Receiver Non-Inverted Data.	
30		GND	Module Ground.	
31		GND	Module Ground.	
32	CML-O	Rx2+	Receiver Non-Inverted Data.	
33	CML-O	Rx2-	Receiver Inverted Data.	
34		GND	Module Ground.	
35	CML-O	Rx4+	Receiver Non-Inverted Data.	

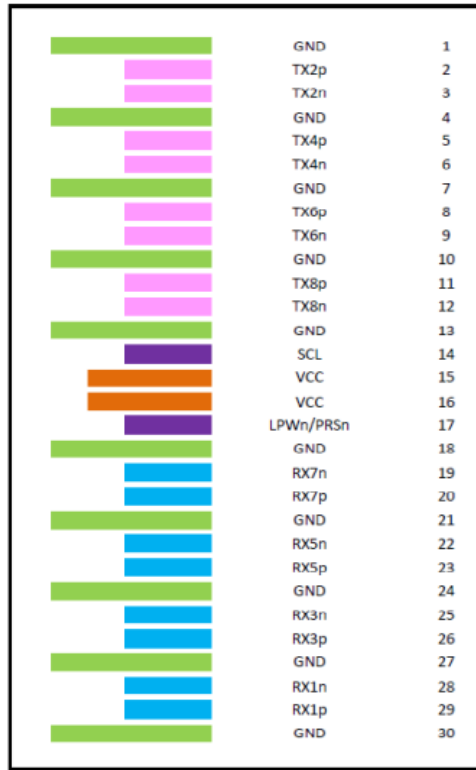
36	CML-O	Rx4-	Receiver Inverted Data.	
37		GND	Module Ground.	
38	CML-O	Rx6+	Receiver Non-Inverted Data.	
39	CML-O	Rx6-	Receiver Inverted Data.	
40		GND	Module Ground.	
41	CML-O	Rx8+	Receiver Non-Inverted Data.	
42	CML-O	Rx8-	Receiver Inverted Data.	
43		GND	Module Ground.	
44	Multi-Level	INT/RSTn	Module Input/Module Reset.	
45		Vcc	+3.3V Power Supply.	
46		Vcc	+3.3V Power Supply.	
47	LVC MOS-I/O	SDA	2-Wire Serial Interface Data.	
48		GND	Module Ground.	
49	CML-I	Tx7-	Transmitter Inverted Data.	
50	CML-I	Tx7+	Transmitter Non-Inverted Data.	
51		GND	Module Ground.	
52	CML-I	Tx5-	Transmitter Inverted Data.	
53	CML-I	Tx5+	Transmitter Non-Inverted Data.	
54		GND	Module Ground.	
55	CML-I	Tx3-	Transmitter Inverted Data.	
56	CML-I	Tx3+	Transmitter Non-Inverted Data.	
57		GND	Module Ground.	
58	CML-I	Tx1-	Transmitter Inverted Data.	
59	CML-I	Tx1+	Transmitter Non-Inverted Data.	
60		GND	Module Ground.	

Electrical Pad Layout

Top Side (viewed from top)

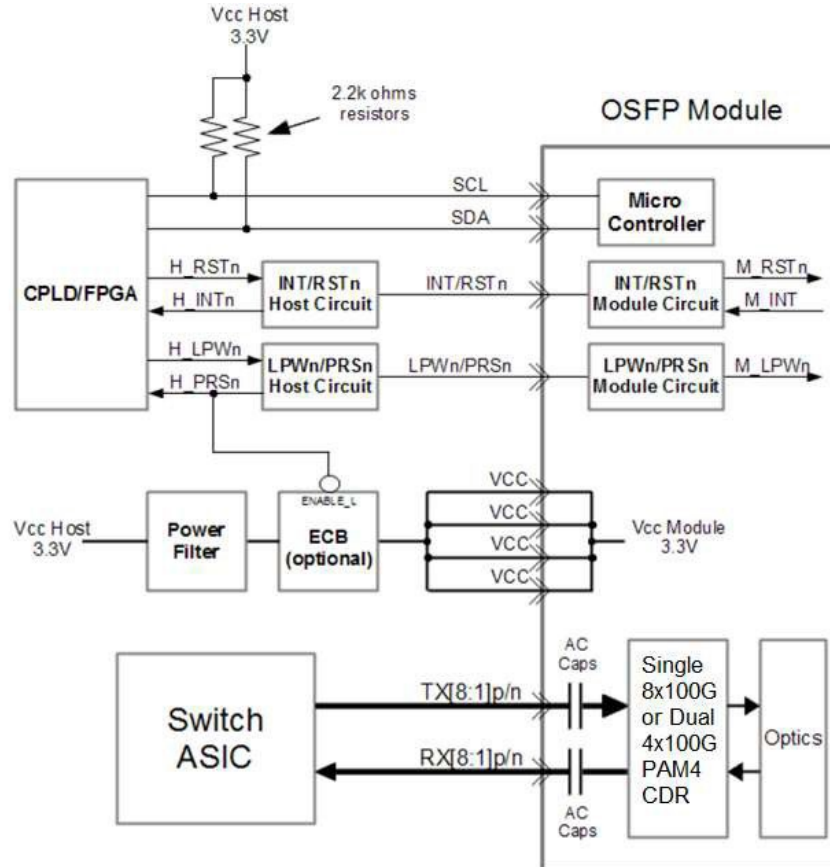


Bottom Side (viewed from bottom)

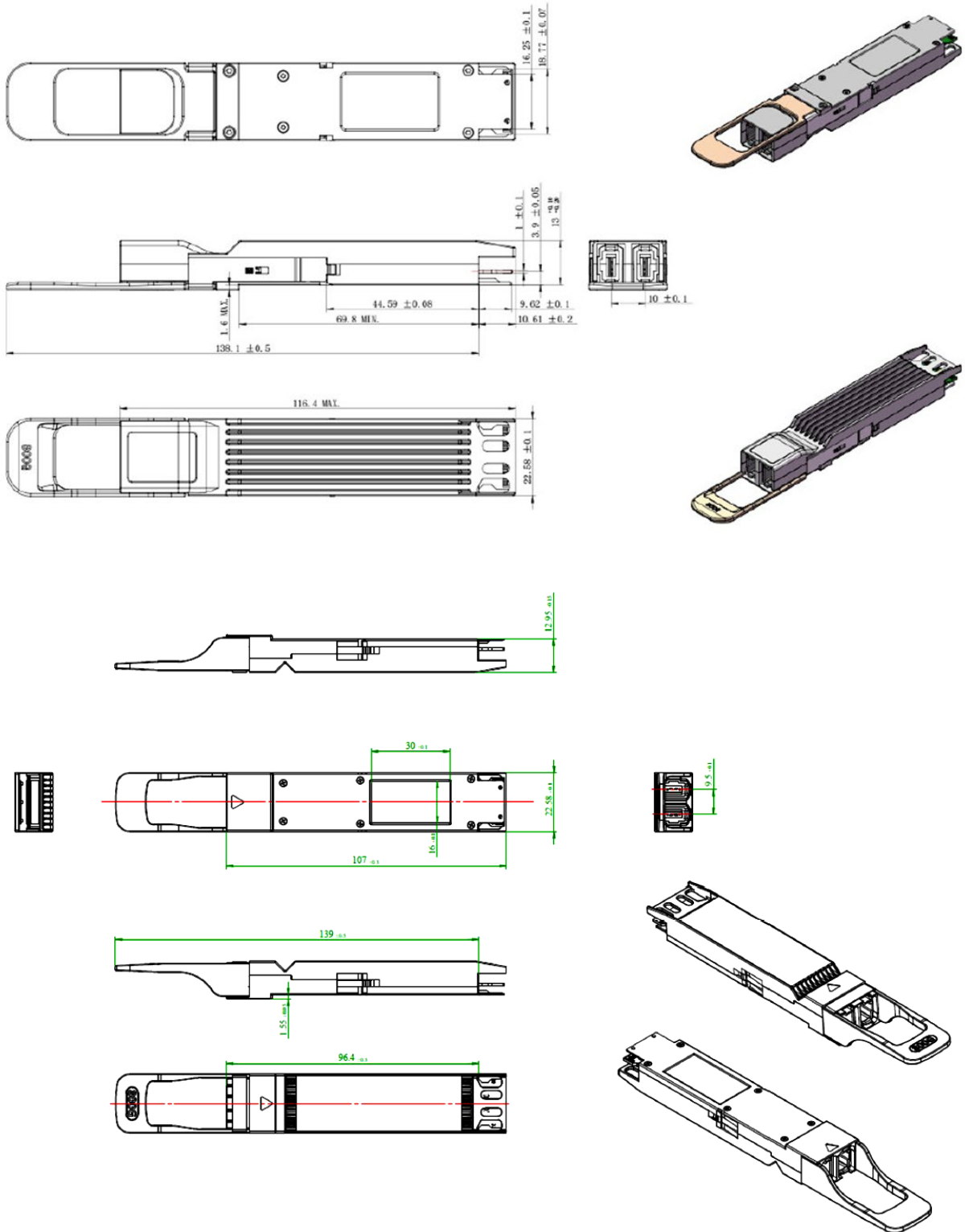


----- Module Card Edge -----

Recommended OSFP Host board Schematic



Mechanical Specifications



*Note: Both Heat Sink Exposed and Heat Sink Enclosed styles are OSFP Type 2 Compliant. Images are for Illustration purposes only. Product Labels, colors, and style may vary.

About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.



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