

## FTCD4533E2PCM-AO

Finisar® Compatible TAA 400GBase-DR4+ QSFP-DD Transceiver (SMF, 1310nm, MPO, 2km, DOM)

### Features

- Compliant with IEEE 802.3bs Standard: 400GAUI-8 Electrical Interface
- Compliant with QSFP-DD MSA HW Rev. 5.1 Type 2 Housing with MPO-12 Connector
- Compliant with IEEE 802.3cu Standard: 4x100GBASE-FR1 Optical Interface
- Maximum Power Consumption: 9W
- 2-Wire Serial Interface with Digital Diagnostic Monitoring
- Compliant with QSFP-DD CMIS Rev. 4.0
- Class 1 Laser
- Complies with EU Directive 2011/65/EU
- RoHS Compliant and Lead-Free
- Operating Temperature: 0 to 70 Celsius



### Applications

- 400GBASE-DR4+
- Access, Metro and Enterprise

### Product Description

This Finisar® compatible QSFP-DD transceiver provides 400GBase-DR4+ throughput up to 2km over single-mode fiber (SMF) using a wavelength of 1310nm via an MPO connector. It is guaranteed to be 100% compatible with the equivalent Finisar® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S.-made or designated country end products."



## Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Storage Temperature	T <sub>stg</sub>	-40		85	°C	
Operating Case Temperature	T <sub>c</sub>	0		70	°C	
Power Supply Voltage	V <sub>cc</sub>	-0.5		3.6	V	
Relative Humidity	RH	5		95	%	
Operating Distance	D	2		2000	m	
Signaling Rate Per Lane	SRL		53.125		GBd	1
Maximum Power Dissipation	PD			9	W	
Maximum Power Dissipation (Low-Power Mode)	PDLP			1.5	W	

### Notes:

1. PAM4.

## Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Supply Voltage	V <sub>cc</sub>	3.135	3.3	3.465	V	
Control Input Voltage	V <sub>I</sub>	-0.3		V <sub>cc</sub> +0.5	V	
Instantaneous Peak Current at Hot Plug	I <sub>cc_IP</sub>			3600	mA	
Sustained Peak Current at Hot Plug	I <sub>cc_SP</sub>			2970	mA	
Power Supply Noise Tolerance (10Hz-10MHz)				66	mV	
Rx Differential Data Output Load			100		Ω	
2-Wire Serial Interface Clock Rate				400	kHz	
<b>Transmitter (Module Input)</b>						
Differential Pk-Pk Input Voltage Tolerance		900			mV	
Differential Termination Mismatch				10	%	
Single-Ended Voltage Tolerance Range		-0.4		3.3	V	
DC Common-Mode Voltage		-350		2850	mV	
<b>Receiver (Module Output)</b>						
AC Common-Mode Output Voltage (RMS)				17.5	mV	
Differential Output Voltage				900	mV	
Near-End Eye Height (Differential)		70			mV	
Far-End Eye Height (Differential)		30			mV	
Far-End Pre-Cursor Ratio		-4.5		2.5	%	
Differential Termination Mismatch				10	%	
Transition Time (Minimum, 20-80%)		9.5			ps	
DC Common-Mode Voltage		-350		2850	mV	
<b>Low-Speed Signal</b>						
Module Output SCL and SDA	V <sub>OL</sub>	0		0.4	V	

Module Input SCL and SDA	VIL	-0.3		Vcc*0.3	V	
	VIH	Vcc*0.7		Vcc+0.5	V	
InitMode, ResetL, and ModSelL	VIL	-0.3		0.8	V	
	VIH	2		Vcc+0.3	V	
IntL	VOL	0		0.4	V	
	VOH	Vcc-0.5		Vcc+0.3	V	

## Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
<b>Transmitter</b>						
Wavelength	$\lambda_C$	1304.5	1311	1317.5	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power Per Lane	AOPL	-3.1		4	dBm	1
Outer Optical Modulation Amplitude (OMA <sub>outer</sub> ) Per Lane	TOMA			4.2	dBm	
Outer Optical Modulation Amplitude (OMA <sub>outer</sub> ) Per Lane	TDECQ < 1.4dB	TOMA	-0.1		dBm	
	1.4dB ≤ TDECQ ≤ 3.4dB		-1.5+TDECQ			
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ) Per Lane	TDECQ			3.4	dB	
Transmitter Eye Closure for PAM4 (TECQ)	TECQ			3.4	dB	
TDECQ - TECQ				2.5	dB	
Over/Under-Shoot				22	%	
Transmitter Power Excursion				2	dBm	
Average Launch Power of Off Transmitter Per Lane	Poff			-15	dBm	
Extinction Ratio Per Lane	ER	3.5			dB	
RIN <sub>17.1</sub> OMA	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	ORL			17.1	dB	
Transmitter Reflectance	TR			-26	dB	
Transmitter Transition Time				17	ps	
<b>Receiver</b>						
Wavelength	$\lambda_C$	1304.5	1311	1317.5	nm	
Damage Threshold Per Lane	AOPD	5			dBm	
Average Receive Power Per Lane	AOPR	-7.1		4	dBm	2
Receive Power (OMA <sub>outer</sub> ) Per Lane	OMAR			4.2	dBm	
Receiver Reflectance	RR			-26	dB	
Receiver Sensitivity (OMA <sub>outer</sub> ) Per Lane	TECQ < 1.4dB	SOMA		-4.5	dBm	
	1.4dB ≤ TECQ ≤ 3.4dB			-5.9+TECQ		
Stressed Receiver Sensitivity (OMA <sub>outer</sub> ) Per Lane	SRS			-2.5	dBm	3
<b>Conditions of Stressed Receiver Sensitivity Test</b>						
Stressed Eye Closure for PAM4 (SECQ)			3.4		dB	

**Notes:**

1. Average launch power, per lane (minimum), is informative and not the principal indicator of signal strength.
2. Average receive power, per lane (minimum), is informative and not the principal indicator of signal strength.
3. Measured with conformance test signal at TP3 for the BER =  $2.4 \times 10^{-4}$ .

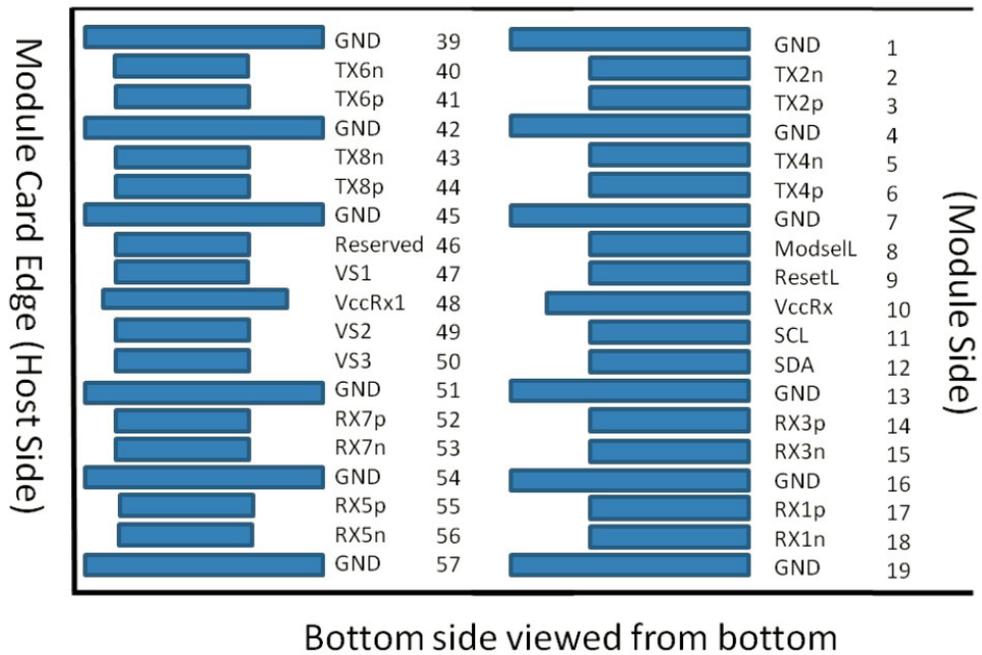
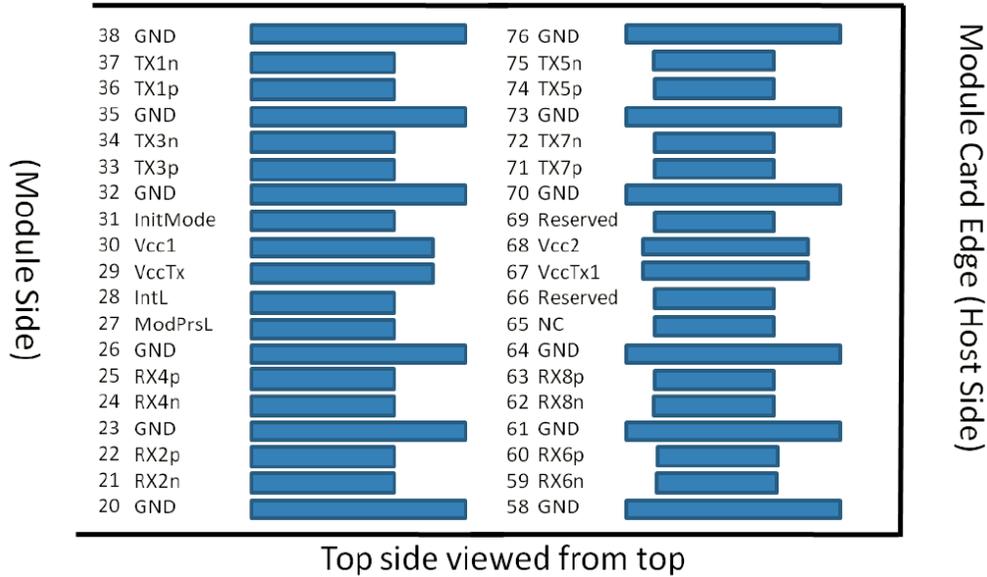
**Pin Description**

Pin	Logic	Symbol	Name/Description	Notes
1		GND	Module Ground.	
2	CML-I	Tx2n	Transmitter Inverted Data Input.	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input.	
4		GND	Module Ground.	
5	CML-I	Tx4n	Transmitter Inverted Data Input.	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input.	
7		GND	Module Ground.	
8	LVTTTL-I	ModSelL	Module Select.	
9	LVTTTL-I	ResetL	Module Reset.	
10		VccRx	+3.3V Receiver Power Supply.	
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock.	
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data.	
13		GND	Module Ground.	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output.	
15	CML-O	Rx3n	Receiver Inverted Data Output.	
16		GND	Module Ground.	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output.	
18	CML-O	Rx1n	Receiver Inverted Data Output.	
19		GND	Module Ground.	
20		GND	Module Ground.	
21	CML-O	Rx2n	Receiver Inverted Data Output.	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output.	
23		GND	Module Ground.	
24	CML-O	Rx4n	Receiver Inverted Data Output.	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output.	
26		GND	Module Ground.	
27	LVTTTL-O	ModPrsL	Module Present.	
28	LVTTTL-O	IntL	Interrupt.	
29		VccTx	+3.3V Transmitter Power Supply.	
30		Vcc1	+3.3V Power Supply.	
31	LVTTTL-I	InitMode	Initialization Mode.	
32		GND	Module Ground.	

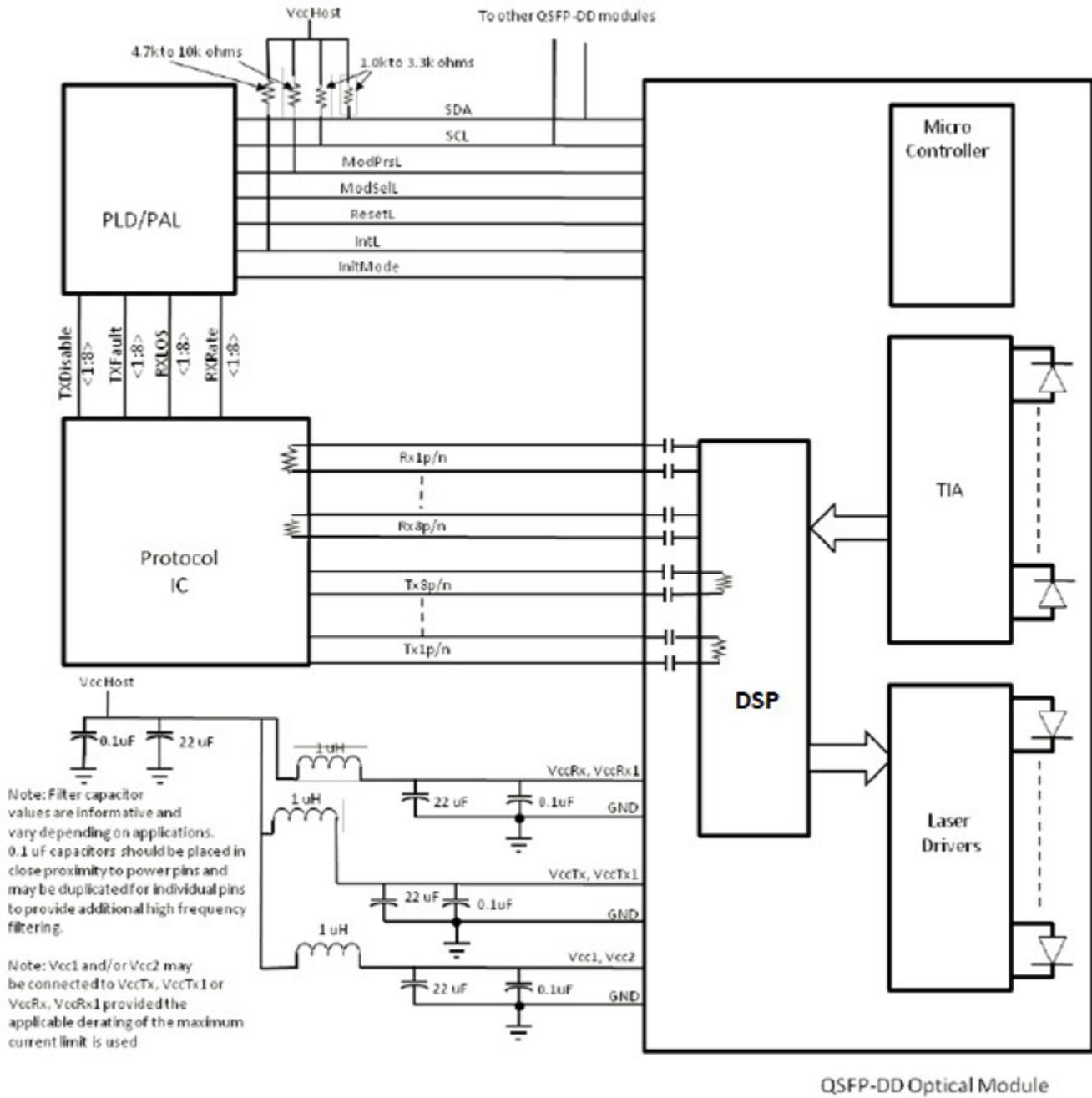
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input.	
34	CML-I	Tx3n	Transmitter Inverted Data Input.	
35		GND	Module Ground.	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input.	
37	CML-I	Tx1n	Transmitter Inverted Data Input.	
38		GND	Module Ground.	
39		GND	Module Ground.	
40	CML-I	Tx6n	Transmitter Inverted Data Input.	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input.	
42		GND	Module Ground.	
43	CML-I	Tx8n	Transmitter Inverted Data Input.	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input.	
45		GND	Module Ground.	
46		Reserved		
47		VS1	Module Vendor-Specific 1.	
48		VccRx1	+3.3V Receiver Power Supply.	
49		VS2	Module Vendor-Specific 2.	
50		VS3	Module Vendor-Specific 3.	
51		GND	Module Ground.	
52	CML-O	Rx7p	Receiver Non-Inverted Data Output.	
53	CML-O	Rx7n	Receiver Inverted Data Output.	
54		GND	Module Ground.	
55	CML-O	Rx5p	Receiver Non-Inverted Data Output.	
56	CML-O	Rx5n	Receiver Inverted Data Output.	
57		GND	Module Ground.	
58		GND	Module Ground.	
59	CML-O	Rx6n	Receiver Inverted Data Output.	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output.	
61		GND	Module Ground.	
62	CML-O	Rx8n	Receiver Inverted Data Output.	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output.	
64		GND	Module Ground.	
65		NC	Not Connected.	
66		Reserved		
67		VccTx1	+3.3V Transmitter Power Supply.	
68		Vcc2	+3.3V Power Supply.	
69		Reserved		
70		GND	Module Ground.	
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input.	
72	CML-I	Tx7n	Transmitter Inverted Data Input.	
73		GND	Module Ground.	

74	CML-I	Tx5p	Transmitter Non-Inverted Data Input.	
75	CML-I	Tx5n	Transmitter Inverted Data Input.	
76		GND	Module Ground.	

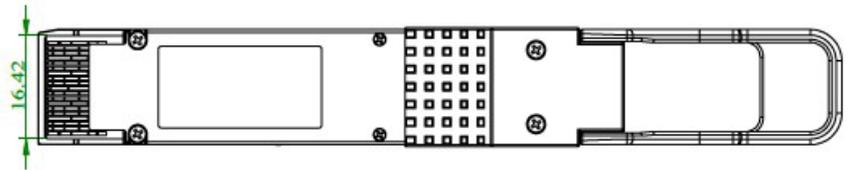
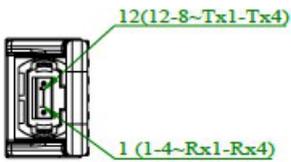
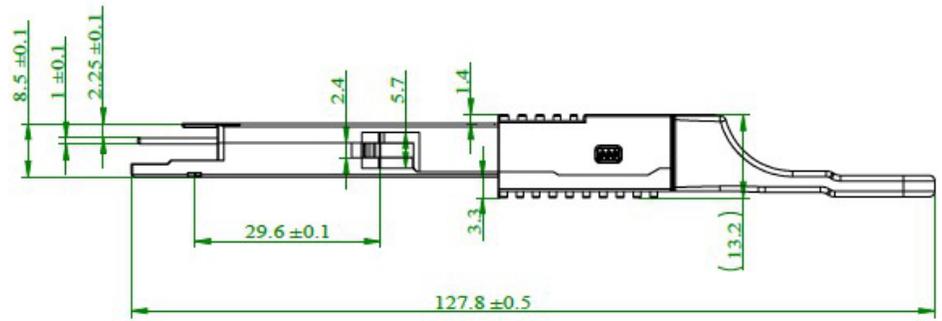
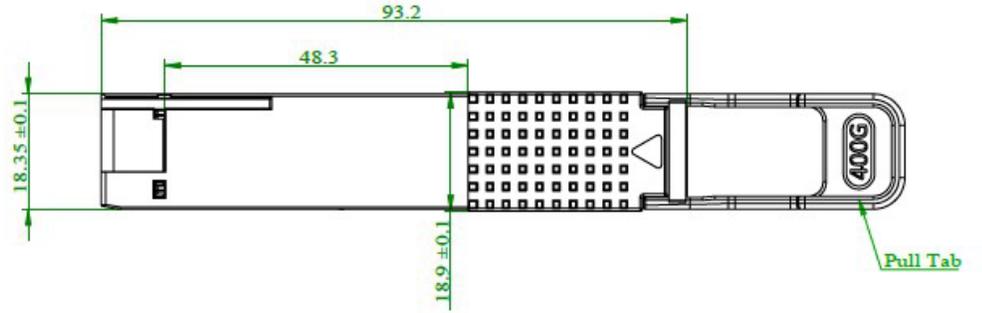
**Electrical Pin-Out Details**



# Recommended QSFP-DD Host Board Schematic



# Mechanical Specifications



## About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.



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