

QSFP28-100GB-SWDM4-AV-AO

ADVA® Compatible 100GBase-SWDM4 QSFP28 Transceiver (MMF, 850nm, 100m, LC, DOM)

Features

- SFF-8665 Compliance
- Duplex LC Connector
- Commercial Temperature 0 to 70 Celsius
- Multi-mode Fiber
- Hot Pluggable
- Excellent ESD Protection
- Metal with Lower EMI
- RoHS Compliant and Lead Free



Applications

- 100GBase Ethernet
- Access and Enterprise

Product Description

This ADVA® QSFP28 transceiver provides 100GBase-SWDM4 throughput up to 100m over OM4 multi-mode fiber (MMF) using a wavelength of 850nm via an LC connector. It is guaranteed to be 100% compatible with the equivalent ADVA® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



Absolute Maximum Ratings

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|-------------------------------------|--------|------|-----|-----|------|-------|
| Maximum Supply Voltage | Vcc | -0.5 | | 3.6 | V | |
| Storage Temperature | TS | -40 | | 85 | °C | |
| Case Operating Temperature | TOP | 0 | | 70 | °C | 1 |
| Relative Humidity | RH | 15 | | 85 | % | 2 |
| Receiver Damage Threshold, per Lane | PRdmg | 3.8 | | | dBm | |

Notes:

1. Temporary excursions case operating temperature of -5 to -75 °C not exceeding 72 hours.
2. Non-condensing.

Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|--|-------------------------------------|-------------------|-----|-------|------|-------|
| Supply Voltage | Vcc | 3.135 | | 3.465 | V | |
| Supply Current | Icc | | | 1.5 | A | |
| Module total power | P | | | 3.5 | W | 1 |
| Transmitter | | | | | | |
| Signaling rate per lane | | 25.78125 ± 100ppm | | | Gb/s | |
| Differential pk-pk input voltage tolerance | Vin,pp,diff | | | 900 | mV | |
| Single-ended voltage tolerance | Vin,pp | -0.35 | | +3.3 | V | |
| Module stress input test | Per Section 83E.3.4.1, IEEE 802.3bm | | | | | |
| Receiver | | | | | | |
| Signaling rate per lane | | 25.78125 ± 100ppm | | | Gb/s | |
| Differential data output swing | Vout,pp | 100 | | 400 | mVpp | 2 |
| | | 300 | | 600 | | |
| | | 400 | 600 | 800 | | |
| | | 600 | | 1200 | | |
| Eye width | | 0.57 | | | UI | |
| Eye height, differential | | 228 | | | mV | |
| Vertical eye closure | VEC | 5.5 | | | dB | |
| Transition time (20% to 80%) | tr, tf | 12 | | | ps | |

Notes:

1. Maximum total power value is specified across the full temperature and voltage range.
2. Output voltage is settable in 4 discrete ranges via I2C. Default range is Range 2 (400 – 800 mV).

Optical Characteristics

| Parameter | Symbol | λ_1 | λ_2 | λ_3 | λ_4 | Unit | Notes |
|--|-----------|-------------|-------------------------------|-------------|-------------|-------|-------|
| Transmitter | | | | | | | |
| Signaling Speed per Lane | | | 25.78125 ± 100ppm | | | Gb/s | 1 |
| Lane center wavelengths (range) | λ | 850 | 880 | 910 | 940 | nm | |
| RMS Spectral Width | SW | 0.59 | 0.59 | 0.59 | 0.59 | nm | |
| Tx _{OMA} min at max TDEC | | -3 | -3 | -3 | -2.9 | dBm | |
| TDEC (OM3) | TDEC | 3.3 | 3.5 | 3.7 | 4.2 | dB | |
| Tx _{OMA} - TDEC | P-TDEC | -6.3 | -6.5 | -6.7 | -7.1 | dBm | |
| Tx _{OMA} min | TxOMA | -5.5 | -5.5 | -5.5 | -5.5 | dBm | |
| Relative Intensity Noise | RIN | | -130 | | | dB/Hz | 2 |
| Optical Extinction Ratio | ER | 2 | 2 | 2 | 2 | dB | |
| Optical Return Loss Tolerance | ORL | | 12 | | | dB | |
| Average launch power of OFF transmitter, per lane | | | -30 | | | dBm | |
| Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3} | | | {0.3,0.38,0.45,0.35,0.41,0.5} | | | | 3 |
| Receiver | | | | | | | |
| Signaling Speed per Lane | | | 25.78125 ± 100ppm | | | GBd | 4 |
| Lane center wavelengths (range) | λ | 850 | 880 | 910 | 940 | nm | |
| Damage Threshold | DT | 3.8 | 3.8 | 3.8 | 3.8 | dBm | |
| Average Receive Power per Lane (min) | RXPmin | -9.5 | -9.4 | -9.4 | -9.4 | dBm | |
| Average Receive Power per Lane (max) | RXPmax | 3.4 | 3.4 | 3.4 | 3.4 | dBm | |
| Receiver Reflectance (max) | Rfl | | -12 | | | dB | |
| Stressed Receiver Sensitivity (OMA) per Lane | SRS | -5.2 | -5.2 | -5.2 | -5.2 | dBm | 5 |
| Back to Back Receiver Sensitivity (OMA) per Lane | RxSens | -8.2 | -8.4 | -8.6 | -8.8 | dBm | 6 |
| Stressed Conditions: | | | | | | | |
| Stressed eye closure | SEC | 3.3 | 3.5 | 3.7 | 4.2 | dB | |
| Stressed eye J2 jitter | J2 | | 0.39 | | | UI | |
| Stressed eye J4 jitter | J4 | | 0.53 | | | UI | |
| Stressed Receiver Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3} | | | {0.28,0.5,0.5,0.33,0.33,0.4} | | | | 7 |
| LOS De-Assert (max) | LOSD | | -11 | | | dBm | 8 |
| LOS Assert (min) | LOSA | | -30 | | | dBm | 8 |
| LOS Hysteresis | | | 0.5 | | | dB | |

Notes:

1. Transmitter consists of 4 lasers and a 4:1 optical multiplexer.
2. Informative, link controlled by TDEC
3. Hit Ratio 1.5×10^{-3} hits/sample.
4. Receiver consists of a 1:4 optical de-multiplexer and 4 photodetectors.
5. 5×10^{-5} BER (pre-FEC).
6. Unstressed receiver sensitivity is information and assumes 5×10^{-5} BER (pre-FEC).
7. Hit Ratio 5×10^{-5} hits/sample.
8. DC values.

Link Budget

| Parameter | Symbol | Min | Typ | Max | Units | Notes |
|-------------------------------------|--------|-----|--------|--------------------|-------|-------|
| Bit Rate (all wavelengths combined) | BR | | 103.10 | | Gb/s | |
| Bit Error Rate | BER | | | 5×10^{-5} | | 1 |
| Insertion Loss | IL | | | 1.8 | dB | 2 |
| Maximum Supported Distances | | | | | | |
| Fiber Type | | | | | | |
| OM3 MMF | Lmax1 | | | 75 | m | 3 |
| OM4 MMF | Lmax2 | | | 100 | m | 3 |
| OM5 MMF | Lmax3 | | | 150 | m | 3 |

Notes:

1. Tested with a $2^{31} - 1$ PRBS at 25.78125 Gb/s
2. 850 nm channel can tolerate 1.9 dB insertion loss
3. Specified at 103.1Gb/s. Requires RS-FEC on the host to support maximum distance.

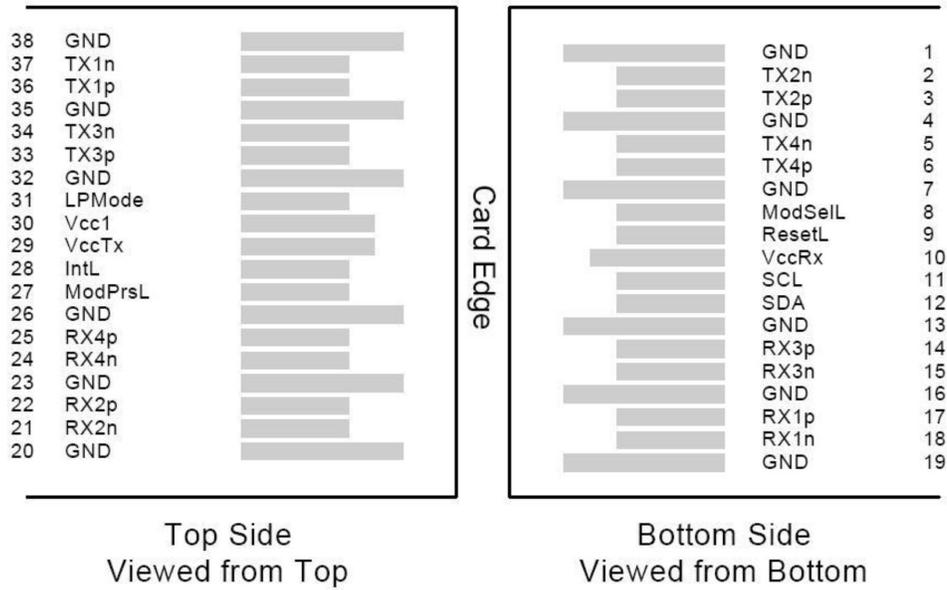
Pin Descriptions

| Pin | Logic | Symbol | Name/Descriptions | Ref. |
|-----|------------|---------|--|------|
| 1 | | GND | Module Ground | 1 |
| 2 | CML-I | Tx2- | Transmitter inverted data input | |
| 3 | CML-I | Tx2+ | Transmitter non-inverted data input | |
| 4 | | GND | Module Ground | 1 |
| 5 | CML-I | Tx4- | Transmitter inverted data input | |
| 6 | CML-I | Tx4+ | Transmitter non-inverted data input | |
| 7 | | GND | Module Ground | 1 |
| 8 | LVTTTL-I | MODSEIL | Module Select | 2 |
| 9 | LVTTTL-I | ResetL | Module Reset | 2 |
| 10 | | VCCRx | +3.3v Receiver Power Supply | |
| 11 | LVCMOS-I | SCL | 2-wire Serial interface clock | 2 |
| 12 | LVCMOS-I/O | SDA | 2-wire Serial interface data | 2 |
| 13 | | GND | Module Ground | 1 |
| 14 | CML-O | RX3+ | Receiver non-inverted data output | |
| 15 | CML-O | RX3- | Receiver inverted data output | |
| 16 | | GND | Module Ground | 1 |
| 17 | CML-O | RX1+ | Receiver non-inverted data output | |
| 18 | CML-O | RX1- | Receiver inverted data output | |
| 19 | | GND | Module Ground | 1 |
| 20 | | GND | Module Ground | 1 |
| 21 | CML-O | RX2- | Receiver inverted data output | |
| 22 | CML-O | RX2+ | Receiver non-inverted data output | |
| 23 | | GND | Module Ground | 1 |
| 24 | CML-O | RX4- | Receiver inverted data output | |
| 25 | CML-O | RX4+ | Receiver non-inverted data output | |
| 26 | | GND | Module Ground | 1 |
| 27 | LVTTTL-O | ModPrsL | Module Present, internal pulled down to GND | |
| 28 | LVTTTL-O | IntL | Interrupt output should be pulled up on host board | 2 |
| 29 | | VCCTx | +3.3v Transmitter Power Supply | |
| 30 | | VCC1 | +3.3v Power Supply | |
| 31 | LVTTTL-I | LPMode | Low Power Mode | 2 |
| 32 | | GND | Module Ground | 1 |
| 33 | CML-I | Tx3+ | Transmitter non-inverted data input | |
| 34 | CML-I | Tx3- | Transmitter inverted data input | |
| 35 | | GND | Module Ground | 1 |
| 36 | CML-I | Tx1+ | Transmitter non-inverted data input | |
| 37 | CML-I | Tx1- | Transmitter inverted data input | |
| 38 | | GND | Module Ground | 1 |

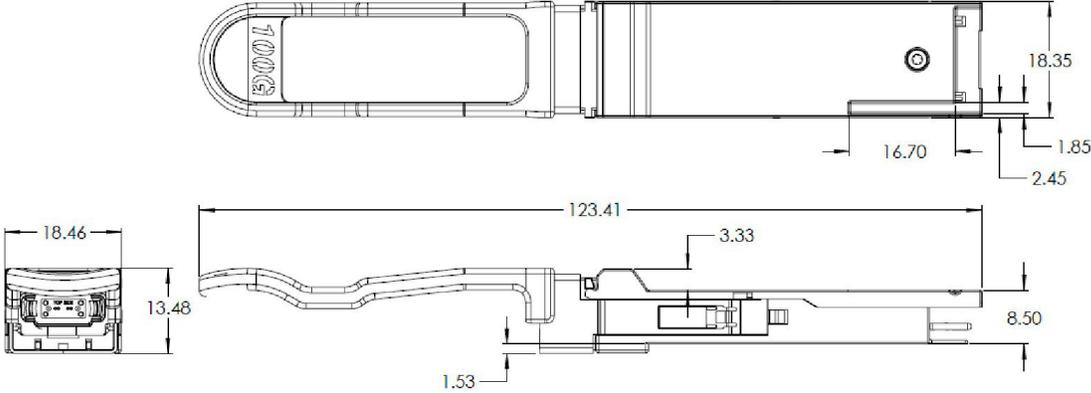
Notes:

1. Module circuit ground is isolated from module chassis ground with in the module.
2. Open collector; should be pulled up with 4.7k-10k ohms on host board to a voltage between 3.15V and 3.6V.

Electrical Pin-out Details



Mechanical Specifications



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.



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