

SFP-10GB-DW-C-H-IF-AO

Infinera® Compatible TAA 10GBase-DWDM SFP+ Transceiver (SMF, Tunable, 80km, LC, DOM, -40 to 92C, Up to Ch.63)

Features

- 50GHz ITU-Based Channel Spacing (C-Band)
- Data Rate 1.2Gbps to 11.3Gbps
- Auto-Tunable
- APD Receiver with Limiting Amplifier
- Low Power Consumption Maximum: 2.3W
- Supports 80km Link Distances
- Power Supply Lines: 3.3V
- Negative Chirp Transmitter with ILMZ (Integrated Laser Mach Zehnder) TOSA
- RoHS Compliant and Lead-Free
- Operating Temperature: -40 to 92 Celsius



Applications

- 8x/10x Fibre Channel
- 10x Gigabit Ethernet over DWDM

Product Description

This Infinera® SFP+ transceiver provides 10GBase-DWDM throughput up to 80km over single-mode fiber (SMF) using a tunable wavelength via an LC connector. It is guaranteed to be 100% compatible with the equivalent Infinera® transceiver. This easy to install, hot swappable transceiver has been programmed, uniquely serialized and data-traffic and application tested to ensure that it will initialize and perform identically. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



ITU Channel Wavelength Guide

| ITU Channel | Frequency (THz) | Center Wavelength (nm) | ITU Channel | Frequency (THz) | Center Wavelength (nm) |
|-------------|-----------------|------------------------|-------------|-----------------|------------------------|
| 13.5 | 191.35 | 1566.72 | 39 | 193.90 | 1546.12 |
| 14 | 191.40 | 1566.31 | 39.5 | 193.95 | 1545.72 |
| 14.5 | 191.45 | 1565.90 | 40 | 194.00 | 1545.32 |
| 15 | 191.50 | 1565.50 | 40.5 | 194.05 | 1544.92 |
| 15.5 | 191.55 | 1565.09 | 41 | 194.10 | 1544.53 |
| 16 | 191.60 | 1564.68 | 41.5 | 194.15 | 1544.13 |
| 16.5 | 191.65 | 1564.27 | 42 | 194.20 | 1543.73 |
| 17 | 191.70 | 1563.86 | 42.5 | 194.25 | 1543.33 |
| 17.5 | 191.75 | 1563.45 | 43 | 194.30 | 1542.94 |
| 18 | 191.80 | 1563.05 | 43.5 | 194.35 | 1542.54 |
| 18.5 | 191.85 | 1562.64 | 44 | 194.40 | 1542.14 |
| 19 | 191.90 | 1562.23 | 44.5 | 194.45 | 1541.75 |
| 19.5 | 191.95 | 1561.83 | 45 | 194.50 | 1541.35 |
| 20 | 192.00 | 1561.42 | 45.5 | 194.55 | 1540.95 |
| 20.5 | 192.05 | 1561.01 | 46 | 194.60 | 1540.56 |
| 21 | 192.10 | 1560.61 | 46.5 | 194.65 | 1540.16 |
| 21.5 | 192.15 | 1560.20 | 47 | 194.70 | 1539.77 |
| 22 | 192.20 | 1559.79 | 47.5 | 194.75 | 1539.37 |
| 22.5 | 192.25 | 1559.39 | 48 | 194.80 | 1538.98 |
| 23 | 192.30 | 1558.98 | 48.5 | 194.85 | 1538.58 |
| 23.5 | 192.35 | 1558.58 | 49 | 194.90 | 1538.19 |
| 24 | 192.40 | 1558.17 | 49.5 | 194.95 | 1537.79 |
| 24.5 | 192.45 | 1557.77 | 50 | 195.00 | 1537.40 |
| 25 | 192.50 | 1557.36 | 50.5 | 195.05 | 1537.00 |
| 25.5 | 192.55 | 1556.96 | 51 | 195.10 | 1536.61 |
| 26 | 192.60 | 1556.56 | 51.5 | 195.15 | 1536.22 |
| 26.5 | 192.65 | 1556.15 | 52 | 195.20 | 1535.82 |
| 27 | 192.70 | 1555.75 | 52.5 | 195.25 | 1535.43 |
| 27.5 | 192.75 | 1555.34 | 53 | 195.30 | 1535.04 |
| 28 | 192.80 | 1554.94 | 53.5 | 195.35 | 1534.64 |
| 28.5 | 192.85 | 1554.54 | 54 | 195.40 | 1534.25 |
| 29 | 192.90 | 1554.13 | 54.5 | 195.45 | 1533.86 |
| 29.5 | 192.95 | 1553.73 | 55 | 195.50 | 1533.47 |
| 30 | 193.00 | 1553.33 | 55.5 | 195.55 | 1533.07 |
| 30.5 | 193.05 | 1552.93 | 56 | 195.60 | 1532.68 |
| 31 | 193.10 | 1552.52 | 56.5 | 195.65 | 1532.29 |
| 31.5 | 193.15 | 1552.12 | 57 | 195.70 | 1531.90 |
| 32 | 193.20 | 1551.72 | 57.5 | 195.75 | 1531.51 |
| 32.5 | 193.25 | 1551.32 | 58 | 195.80 | 1531.12 |
| 33 | 193.30 | 1550.92 | 58.5 | 195.85 | 1530.72 |
| 33.5 | 193.35 | 1550.52 | 59 | 195.90 | 1530.33 |
| 34 | 193.40 | 1550.12 | 59.5 | 195.95 | 1529.94 |
| 34.5 | 193.45 | 1549.72 | 59.5 | 195.95 | 1529.94 |
| 35 | 193.50 | 1549.32 | 60 | 196.00 | 1529.55 |
| 35.5 | 193.55 | 1548.91 | 60.5 | 196.05 | 1529.16 |
| 36 | 193.60 | 1548.52 | 61 | 196.10 | 1528.77 |
| 36.5 | 193.65 | 1548.11 | 61.5 | 196.15 | 1528.38 |

| | | | | | |
|-------------|--------|---------|-------------|--------|---------|
| 37 | 193.70 | 1547.72 | 62 | 196.20 | 1527.99 |
| 37.5 | 193.75 | 1547.32 | 62.5 | 196.25 | 1527.61 |
| 38 | 193.80 | 1546.92 | 63 | 196.30 | 1527.21 |
| 38.5 | 193.85 | 1546.52 | | | |

Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Unit | Notes |
|----------------------------|--------|------|------|------|---------|
| Maximum Supply Voltage | Vcc | 0 | 3.6 | V | +3.3V |
| Optical Receiver Input | PIMAX | | 5 | dBm | Average |
| Operating Case Temperature | Tc | -40 | 92 | °C | |
| Storage Temperature | Tstg | -40 | 85 | °C | |
| ESD SFI Pins | ESD1 | | 1 | kV | HBM |
| ESD Except for SFI Pins | ESD2 | | 2 | kV | HBM |
| Data Rate | DR | 1.2 | 11.3 | Gbps | NRZ |

Electrical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|---|----------|--------------|------|--------------|------|---|
| Supply Voltage | Vcc | 3.135 | 3.3 | 3.465 | V | 3.3V |
| Supply Current | Icc | | | 0.73 0.86 | A | -40°C to 85°C 86°C to 92°C |
| Power Consumption | | | | 2.3 2.7 | W | -40°C to 85°C 86°C to 92°C |
| Low-Speed Control Pin Logic Levels | | | | | | |
| Host_Vcc Range | Host_Vcc | 3.14 | | 3.47 | V | With ±5% variation |
| Tx_Fault, Rx_LOS | VOL | 0.0 | | 0.4 | V | Note 1 |
| | VOH | Host_Vcc-0.5 | | Host_Vcc+0.3 | V | Note 1 |
| Tx_Disable | VIL | -0.3 | | 0.8 | V | Pulled up with 10kΩ to the VccT in the module |
| | VIH | 2.0 | | VccT+0.3 | V | |

Notes:

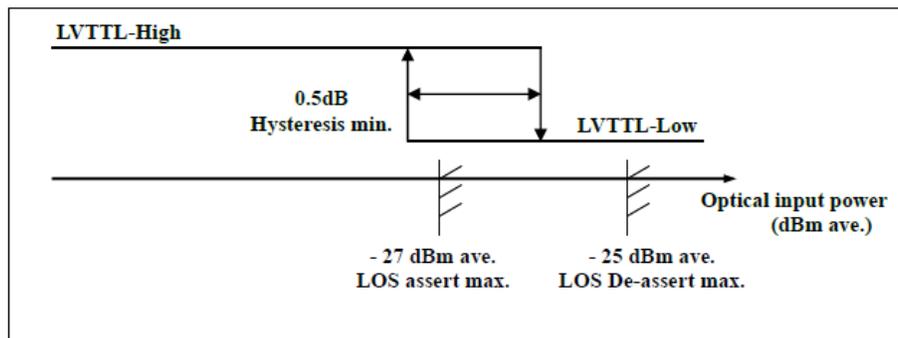
1. Rpullup (Rp) is the pull-up resistor. Active bus termination may be used by the host in place of a pull-up resistor. Pull-ups can be connected to multiple power supplies; however, the host board design shall ensure that no module pin has a voltage exceeding the module. Measures at the host side of the connector.

Optical Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Notes |
|--|-------------------|---------------------|------|--------|------|---|
| SBS Threshold | | 10 | | | dBm | |
| Transmitter | | | | | | |
| Frequency Range | | 191.35 | | 196.30 | THz | 50GHz Grid, 96 Channels |
| Frequency Accuracy | | -2.5 | | 2.5 | GHz | EOL |
| Optical Transmit Power | P _o | -1 | | 3 | dBm | EOL |
| Shuttered Output Power | | | | -35 | dBm | |
| Optical Power Stability | ΔP _o | -1 | | 1 | dB | All Channels, SOL |
| Side-Mode Suppression | SMSR | 35 | | | dB | ±2.5nm, Modulated |
| Spectral Width | Δλ | | 0.3 | 0.5 | nm | -20dB, Modulated |
| Extinction Ratio | ER | 8.2 | | | dB | Filtered, 10.3Gbps |
| Eye Diagram Compliance | | GR-253, ITU-T G.691 | | | | |
| Mask Margin | | 10 | | | % | |
| Tuning Speed | | | | 10 | s | Warmed-Up, From Any CH to Any Other CH |
| Receiver | | | | | | |
| Input Operating Wavelength | | 1525 | | 1575 | nm | |
| Minimum Receiver Sensitivity (Back-to-Back) | P _{rmin} | | | -24 | dBm | 10.709Gbps, 1E ⁻¹² , OSNR>35dB |
| Minimum Receiver Sensitivity (-300~+1400ps/nm) | P _{rmin} | | | -21 | dBm | |
| Maximum Input Power (Overload) | P _{ro} | -7 | | | dBm | |
| Receiver Reflectance | RL | | | -27 | dB | |
| LOS Assert | | -27.5 | | | dBm | Note 1 |
| LOS De-Assert | | | | -24 | dBm | Note 1 |
| LOS Hysteresis | | 0.1 | | | dB | Note 1 |
| LOS Assert Time | | | | 100 | μs | |
| LOS De-Assert Time | | | | 100 | μs | |

Notes:

1.



SFP+ 2-Wire Interface Requirements

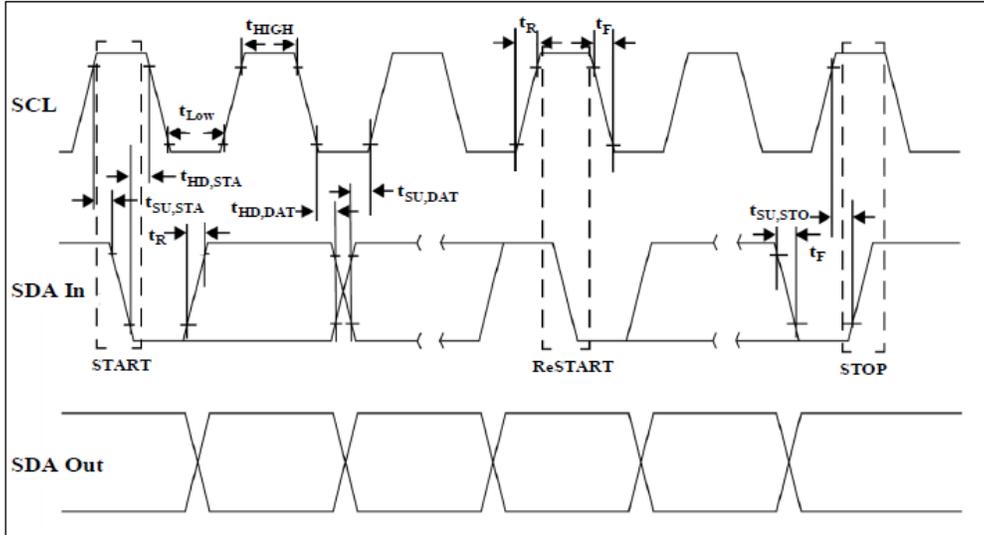
| Parameter | Symbol | Min. | Max. | Unit | Notes/Conditions |
|---|-----------------------------|----------------|----------------|--------|---|
| Timing Requirements | | | | | |
| Clock Frequency | fSCL | 100 | 400 | kHz | |
| Clock Pulse Width - Low | tLOW | 1.3 | | μs | |
| Clock Pulse Width - High | tHIGH | 0.6 | | μs | |
| Time Bus is Free Before a New Transaction Can Start | tBUF | 20 | | μs | Between STOP and START |
| START Hold Time | tHD,STA | 0.6 | | μs | |
| START Set-Up Time | tSU,STA | 0.6 | | μs | |
| Data In Hold Time | tHD,DAT | 0 | | μs | |
| Data In Set-Up Time | tSU,DAT | 0.1 | | μs | |
| Input Rise Time (100kHz) | tR,100 | | 1000 | ns | Note 1 |
| Input Rise Time (400kHz) | tR,400 | | 300 | ns | Note 1 |
| Input Fall Time (100kHz) | tF,100 | | 300 | ns | Note 1 |
| Input Fall Time (400kHz) | tF,400 | | 300 | ns | Note 1 |
| STOP Set-Up Time | tSU,STO | 0.6 | | μs | |
| Serial Interface Clock Hold-Off "Clock Stretching" | T_clock_hold | | 500 | μs | Maximum time the SFP+ may hold the SCL line "low" before continuing R or W operation |
| Complete Single or Sequential Write | tWR | | 40 | ms | Complete (up to) 8-byte write |
| Endurance (Write Cycles) | | 10k | | cycles | @Max. operating temperature |
| Physical Interface | | | | | |
| SCL and SDA | VOL | 0.0 | 0.40 | V | Rpullup ² pulled to Host_Vcc, IOL(max.) = 3mA |
| | VOH | Host_Vcc – 0.5 | Host_Vcc + 0.3 | V | Rpullup ² pulled to Host_Vcc |
| | VIL | -0.3 | VccT * 0.3 | V | |
| | VIH | VccT * 0.7 | VccT + 0.5 | V | |
| Host_Vcc Range | Host_Vcc | 3.14 | 3.47 | V | |
| Input Current on SCL and SDA Pins | IL | -10 | 10 | μA | |
| Capacitance on SCL and SDA Pins | C _i ² | | 14 | pF | |
| Total Bus Capacitance for SCL and SDA | C _b ³ | | 100 | pF | At 400kHz, R _p (max.) = 3.0kΩ At 100kHz, R _p (max.) = 8.0kΩ |
| | | | 290 | pF | At 400kHz, R _p (max.) = 1.1kΩ At 100kHz, R _p (max.) = 2.75kΩ |

Notes:

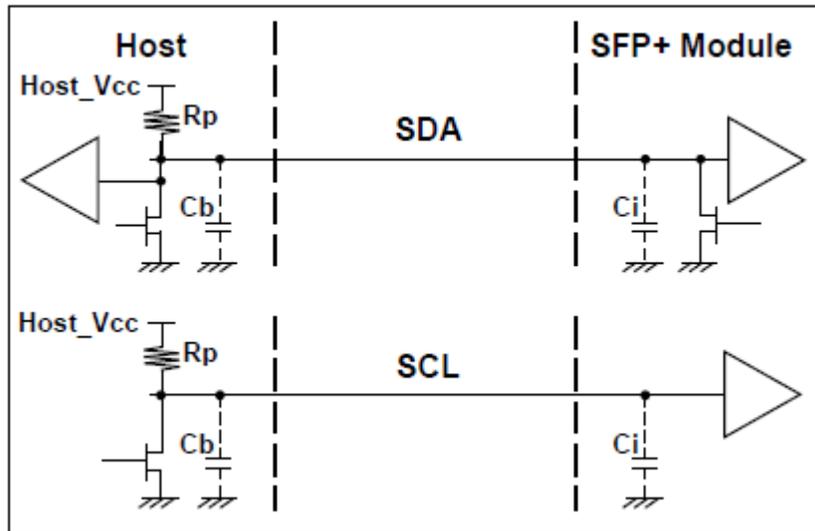
- From (VIL, MAX-0.15) to (VIH, MIN+0.15).
- Rpullup (R_p) is the pull-up resistor. Active bus termination may be used by the host in place of a pull-up resistor. Pull-ups can be connected to multiple power supplies; however, the host board design shall ensure that no module pin has voltage exceeding the module. Measured at the host side of the connector. VccT/R+0.5V nor requires the module to sink more than 3.0mA current.

- 3. C_i is the capacitance looking into the module SCL and SDA pins.
- 4. C_b is the total bus capacitance on the SCL or SDA bus.

SFP+ Timing Diagram



Physical Interface



SFP+ Timing Requirements

| Parameter | Symbol | Min. | Max. | Unit | Notes/Conditions |
|--|--------------------|------|------|------|--|
| Tx_Disable Assert Time | t_off | | 100 | μs | Rising edge of Tx_Disable to fall off output signal below 10% of nominal. |
| Tx_Disable Negate Time | t_on | | 2 | ms | Falling edge of Tx_Disable to rise output signal above 90% of nominal. This only applies in normal operation, not during start-up or fault recovery. |
| Time to Initialize 2-Wire Interface | t_2w_start_up | | 300 | ms | From power on or hot plug after the supply meeting. |
| Time to Initialize Cooled Module and Time to Power Up a Cooled Module to Power Level II | t_start_up_cooled | | 90 | sec | From power supplies meeting or hot plug, or Tx_Disable negated during power up or Tx_Fault recovery, until cooled Power Level II part during fault recovery is fully operational. Also, from stop bit-low-to-high SDA transition enabling Power Level II until the cooled module is fully operational. |
| Tx_Fault Assert for Cooled Module | Tx_fault_on_cooled | | 1 | ms | From occurrence of fault to assertion of Tx_Fault. |
| Tx_Fault Reset | t_reset | 10 | | μs | Time Tx_Disable must be held "high" to reset Tx_Fault. |
| Rx_LOS Assert Delay | t_los_on | | 100 | μs | From occurrence of loss of signal to assertion of Rx_LOS. |
| Rx_LOS Negate Delay | t_los_off | | 100 | μs | From occurrence of presence of signal to negation of Rx_LOS. |
| Maximum Current Ramp on Power Supply | | | | | |
| Icc Instantaneous Peak Current | | | 800 | mA | Notes 1, 2 |
| Icc Sustained Peak Current | | | 660 | mA | Notes 1, 2 |

Notes:

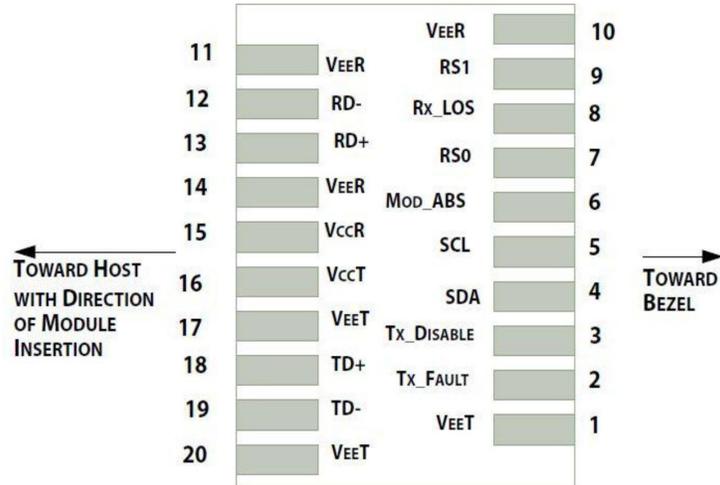
1. The maximum currents are the allowed currents for each power supply (VccT or VccR); therefore, the total module peak currents can be twice this value. The instantaneous peak current is allowed to exceed to specified maximum current capacity of the connector contact for a short period.
2. Not to exceed the sustained peak limit for the more than 50μs. May exceed this limit for shorter durations.

Pin Descriptions

| Pin | Logic | Symbol | Power Sequence Order | Name/Description | Notes |
|-----|------------|------------|----------------------|---|-------|
| 1 | | VeeT | 1 | Module Transmitter Ground. | 1 |
| 2 | LVTTTL-O | Tx_Fault | 3 | Module Transmitter Fault. | 2 |
| 3 | LVTTTL-I | Tx_Disable | 3 | Transmitter Disable. Turn off the laser output. | 3 |
| 4 | LVTTTL-I/O | SDA | 3 | 2-Wire Serial Interface Data. | |
| 5 | LVTTTL-I/O | SCL | 3 | 2-Wire Serial Interface Clock. | |
| 6 | | MOD_ABS | 3 | Module Absent. Connected to the VeeT or VeeR in the module. | 4 |
| 7 | LVTTTL-I | RS0 | 3 | N/A. 30k Ω pull-down inside the module. | |
| 8 | LVTTTL-O | Rx_LOS | 3 | Receiver Loss of Signal Indicator. | 2 |
| 9 | LVTTTL-I | RS1 | 3 | N/A. 30k Ω pull-down inside the module. | |
| 10 | | VeeR | 1 | Module Receiver Ground. | 1 |
| 11 | | VeeR | 1 | Module Receiver Ground. | 1 |
| 12 | CML-O | RD- | 3 | Receiver Inverted Data Output (SFI). | |
| 13 | CML-O | RD+ | 3 | Receiver Non-Inverted Data Output (SFI). | |
| 14 | | VeeR | 1 | Module Receiver Ground. | 1 |
| 15 | | VccR | 2 | 3.3V Module Receiver Supply. | 5 |
| 16 | | VccT | 2 | 3.3V Module Transmitter Supply. | 5 |
| 17 | | VeeT | 1 | Module Transmitter Ground. | 1 |
| 18 | CML-I | TD+ | 3 | Transmitter Non-Inverted Data Output (SFI). | |
| 19 | CML-I | TD- | 3 | Transmitter Inverted Data Output (SFI). | |
| 20 | | VeeT | 1 | Module Transmitter Ground. | 1 |

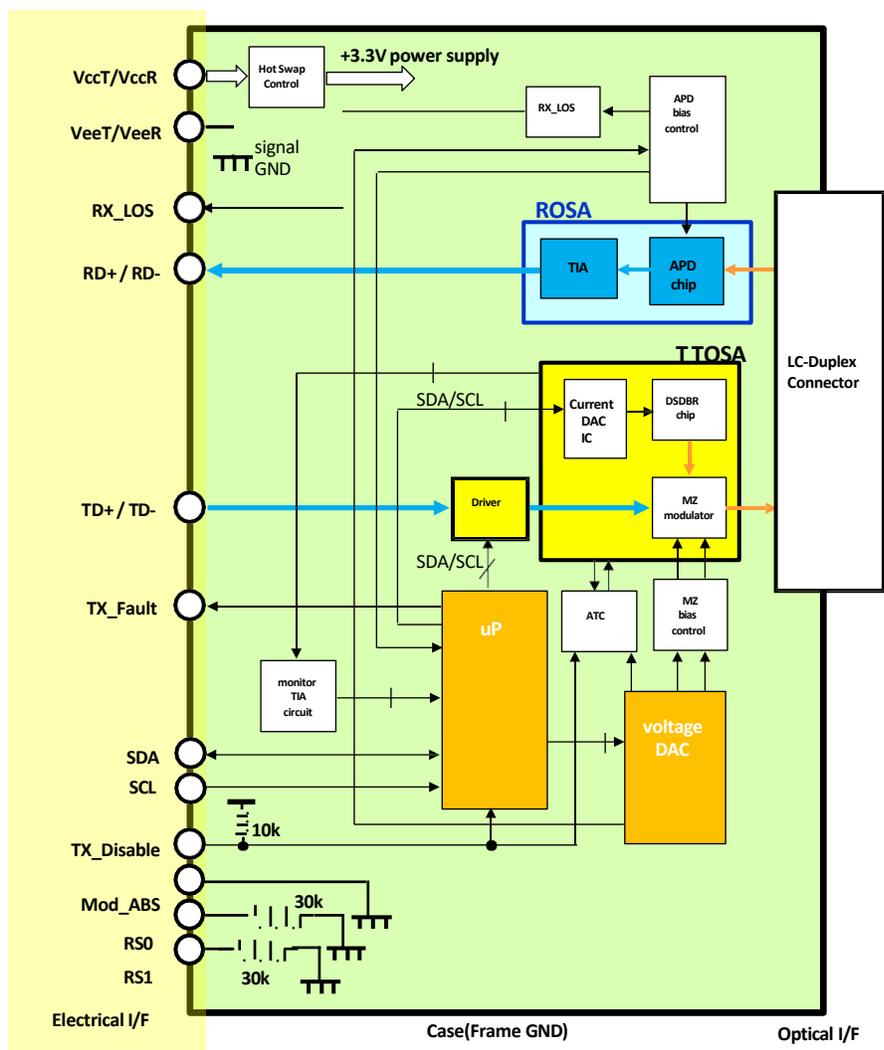
Notes:

1. The module signal ground pins, VeeR and VeeT, are isolated from the module case.
2. This pin is an open drain output pin and shall be pulled up with a 4.7k Ω to 10k Ω to the Host_Vcc on the host board. Pull-ups can be connected to multiple power supplies; however, the host board design shall ensure that no module pin has a voltage exceeding module VccT/R+0.5V.
3. This pin is an input pin with 10k Ω pull-up to the VccT in the module.
4. This pin shall be pulled up with 4.7k Ω to 10k Ω to the Host_Vcc on the host board.
5. VccT and VccR are tied together inside the module.



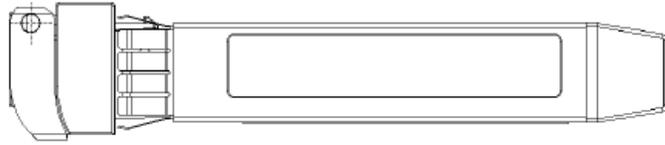
Pin-Out of Connector Block on the Host Board

Recommended Circuit Schematic

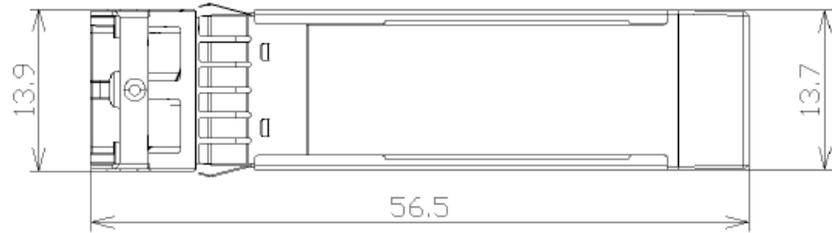
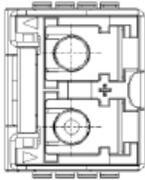


Mechanical Specifications

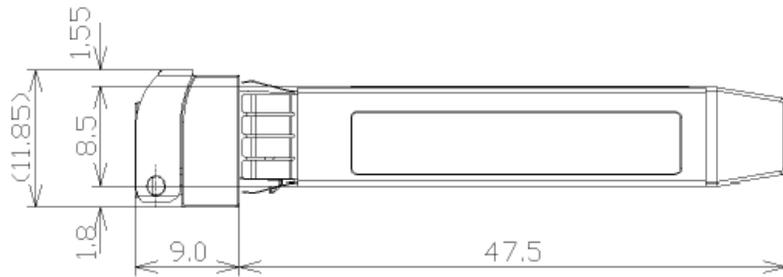
Side view



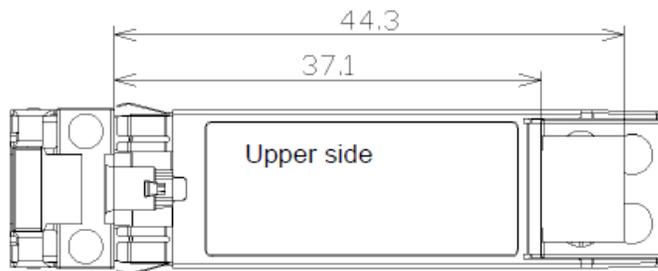
Top view



Side view



Bottom view



About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.



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