

## QDD-200GB-PSM8-AO

MSA and TAA 200GBase-PSM8 QSFP-DD Transceiver (SMF, 1310nm, 2km, MPO-24, DOM)

### Features

- 8 Channels 1310nm DFB
- 8 Channels Full-Duplex Transceiver Modules
- Supports 8x25Gbps and 8x10Gbps Aggregate Bit Rates
- Internal CDR Circuits on Both Receiver and Transmitter Channels
- Supports CDR Bypass
- 8 Channels PIN Photo Detector Array
- Up to 2km Reach for G.652 SMF
- 3.3V Power Supply Voltage
- Operating Temperature: 0 to 70 Celsius
- Hot Pluggable QSFP-DD Form Factor
- RoHS Compliant and Lead-Free



### Applications

- 200G Ethernet

### Product Description

This MSA Compliant QSFP-DD transceiver provides 200GBase-PSM8 throughput up to 2km over single-mode fiber (SMF) using a wavelength of 1310nm via an MPO-24 connector. It is built to MSA standards and is uniquely serialized and data-traffic and application tested to ensure that they will integrate into your network seamlessly. Digital optical monitoring (DOM) support is also present to allow access to real-time operating parameters. This transceiver is Trade Agreements Act (TAA) compliant. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

AddOn's transceivers are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products."



## Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	-0.3		3.6	V	
Input Voltage	VIN	-0.3		Vcc+0.3	V	
Storage Temperature	Tstg	-20		85	°C	
Operating Case Temperature	Tc	0		70	°C	
Relative Humidity (Non-Condensing)	RH	5		95	%	
Data Rate	DR	10.3125	25.78125		Gbps	
Fiber Bend Radius	FBR	0.002		2	km	

## Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Power Supply Voltage	Vcc	3.13	3.3	3.47	V	
Power Dissipation	P <sub>DISS</sub>		5.28	6	W	
Differential Input Impedance	ZIN	90	100	110	Ω	
Differential Output Impedance	ZOUT	90	100	110	Ω	
Differential Input Voltage Amplitude	ΔVIN	190		700	mVp-p	1
Differential Output Voltage Amplitude	ΔVOUT	300		850	mVp-p	2
Input Logic Level - High	VIH	2.0		Vcc	V	
Input Logic Level - Low	VIL	0		0.8	V	
Output Logic Level - High	VOH	Vcc-0.5		Vcc	V	
Output Logic Level - Low	VOL	0		0.4	V	

### Notes:

1. Differential input voltage amplitude is measured between Tx#+ and Tx#-.
2. Differential output voltage amplitude is measured between Rx#+ and Rx#-.

## Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
<b>Transmitter</b>						
Center Wavelength	$\lambda_C$	1295	1310	1325	nm	
Side-Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power Per Lane	Pavg	-6		2	dBm	
Optical Modulation Amplitude Per Lane	POMA	-5.0		2.2	dBm	
TDP Per Lane	TDP			2.9	dB	
Extinction Ratio	ER	3.5			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	RT			-12	dB	
Average Launch Power of Off Transmitter Per Lane	Poff			-30	dB	
Eye Mask Coordinates: (X1, X2, X3, Y1, Y2, Y3)	(0.31, 0.4, 0.45, 0.34, 0.38, 0.4) Hit Ratio = $5 \times 10^{-5}$					
<b>Receiver</b>						
Center Wavelength	$\lambda_C$	1295	1310	1325	nm	
Damage Threshold Per Lane	THd	3.0			dBm	
Average Receive Power Per Lane		-12.66		2.0	dBm	
Maximum Receive Power Per Lane (OMA)				2.2	dBm	
Receiver Reflectance	RR			-26	dBm	
Receiver Sensitivity (OMA) Per Lane	SEN			-11.35	dBm	
LOS Assert	LOSA		-18		dBm	
LOS De-Assert – OMA	LOSD		-15		dBm	
LOS Hysteresis	LOSH	0.5		3	dB	

### Notes:

1. Even if the TDP < 1dB, the OMA minimum must exceed the minimum value specified here.
2. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
3. Sensitivity is specified at  $5 \times 10^{-5}$  BER @ 25.78125Gbps.

## Pin Descriptions

Pin	Symbol	Logic	Name/Description	Plug Sequence	Notes
1	GND		Module Ground.	1B	1
2	Tx2-	CML-I	Transmitter Inverted Data Input.	3B	
3	Tx2+	CML-I	Transmitter Non-Inverted Data Input.	3B	
4	GND		Module Ground.	1B	1
5	Tx4-	CML-I	Transmitter Inverted Data Input.	3B	
6	Tx4+	CML-I	Transmitter Non-Inverted Data Input.	3B	
7	GND		Module Ground.	1B	1
8	ModSelL	LVTTTL-I	Module Select.	3B	
9	ResetL	LVTTTL-I	Module Reset.	3B	
10	VccRx		+3.3V Receiver Power Supply.	2B	2
11	SCL	LVCNOS-I/O	2-Wire Serial Interface Clock.	3B	
12	SDA	LVCNOS-I/O	2-Wire Serial Interface Data.	3B	
13	GND		Module Ground.	1B	1
14	Rx3+	CML-O	Receiver Non-Inverted Data Input.	3B	
15	Rx3-	CML-O	Receiver Inverted Data Input.	3B	
16	GND		Module Ground.	1B	1
17	Rx1+	CML-O	Receiver Non-Inverted Data Input.	3B	
18	Rx1-	CML-O	Receiver Inverted Data Input.	3B	
19	GND		Module Ground.	1B	1
20	GND		Module Ground.	1B	1
21	Rx2-	CML-O	Receiver Inverted Data Input.	3B	
22	Rx2+	CML-O	Receiver Non-Inverted Data Input.	3B	
23	GND		Module Ground.	1B	1
24	Rx4-	CML-O	Receiver Inverted Data Input.	3B	
25	Rx4+	CML-O	Receiver Non-Inverted Data Input.	3B	
26	GND		Module Ground.	1B	2
27	ModPrsL	LVTTTL-O	Module Present.	3B	2
28	IntL	LVTTTL-O	Interrupt.	3B	
29	VccTx		+3.3V Transmitter Power Supply.	2B	1
30	Vcc1		+3.3V Power Supply.	2B	
31	InitMode	LVTTTL-I	Initialization Mode. In legacy QSFP applications, the InitMode pad is called LPMODE.	3B	
32	GND		Module Ground.	1B	1
33	Tx3+	CML-I	Transmitter Non-Inverted Data Input.	3B	
34	Tx3-	CML-I	Transmitter Inverted Data Input.	3B	
35	GND		Module Ground.	1B	1
36	Tx1+	CML-I	Transmitter Non-Inverted Data Input.	3B	

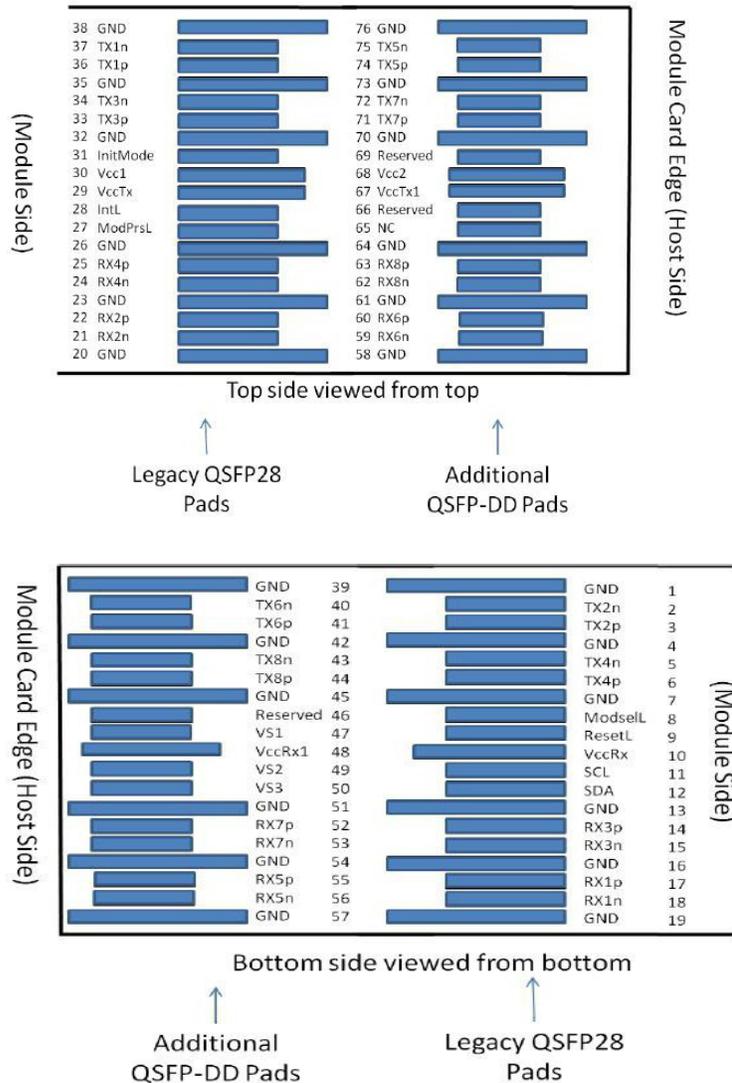
37	Tx1-	CML-I	Transmitter Inverted Data Input.	3B	
38	GND		Module Ground.	1B	1
39	GND		Module Ground.	1A	1
40	Tx6-	CML-I	Transmitter Inverted Data Input.	3A	
41	Tx6+	CML-I	Transmitter Non-Inverted Data Input.	3A	
42	GND		Module Ground.	1A	1
43	Tx8-	CML-I	Transmitter Inverted Data Input.	3A	
44	Tx8+	CML-I	Transmitter Non-Inverted Data Input.	3A	
45	GND		Module Ground.	1A	1
46	Reserved		For Future Use.	3A	3
47	VS1		Module Vendor-Specific 1.	3A	3
48	VccRx1		+3.3V Receiver Power Supply.	2A	2
49	VS2		Module Vendor-Specific 2.	3A	3
50	VS3		Module Vendor-Specific 3.	3A	3
51	GND		Module Ground.	1A	1
52	Rx7+	CML-O	Receiver Non-Inverted Data Input.	3A	
53	Rx7-	CML-O	Receiver Inverted Data Input.	3A	
54	GND		Module Ground.	1A	1
55	Rx5+	CML-O	Receiver Non-Inverted Data Input.	3A	
56	Rx5-	CML-O	Receiver Inverted Data Input.	3A	
57	GND		Module Ground.	1A	1
58	GND		Module Ground.	1A	1
59	Rx6-	CML-O	Receiver Inverted Data Input.	3A	
60	Rx6+	CML-O	Receiver Non-Inverted Data Input.	3A	
61	GND		Module Ground.	1A	1
62	Rx8-	CML-O	Receiver Inverted Data Input.	3A	
63	Rx8+	CML-O	Receiver Non-Inverted Data Input.	3A	
64	GND		Module Ground.	1A	1
65	NC		Not Connected.	3A	3
66	Reserved		For Future Use.	3A	3
67	VccTx1		+3.3V Transmitter Power Supply.	2A	2
68	Vcc2		+3.3V Power Supply.	2A	2
69	Reserved		For Future Use.	3A	3
70	GND		Module Ground.	1A	1
71	Tx7+	CML-I	Transmitter Non-Inverted Data Input.	3A	
72	Tx7-	CML-I	Transmitter Inverted Data Input.	3A	
73	GND		Module Ground.	1A	1
74	Tx5+	CML-I	Transmitter Non-Inverted Data Input.	3A	

75	Tx5-	CML-I	Transmitter Inverted Data Input.	3A	
76	GND		Module Ground.	1A	1

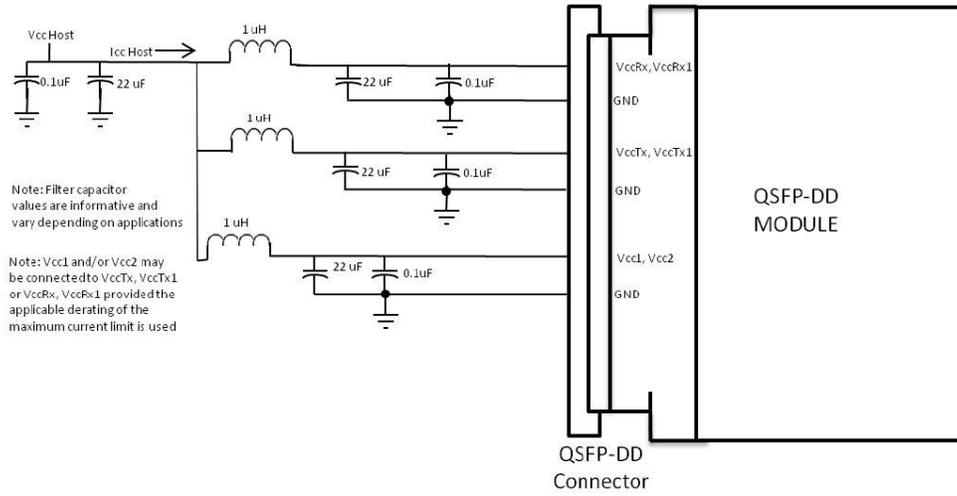
**Notes:**

1. QSFP-DD uses common ground (GND) for all signals and supply power. All are common within the QSFP-DD module, and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 shall be applied concurrently. VccRx, VccRx1, Vcc1, Vcc2, VccTx, and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 100mA.
3. All Vendor-Specific, Reserved, and Not Connected pins may be terminated with 50Ω to ground on the host. Pad 65 (Not Connected) shall be left unconnected within the module. Vendor-Specific and Reserved pads shall have an impedance to GND that is greater than 10kΩ and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, and 3B. Contact Sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, and by 3A, 3B.

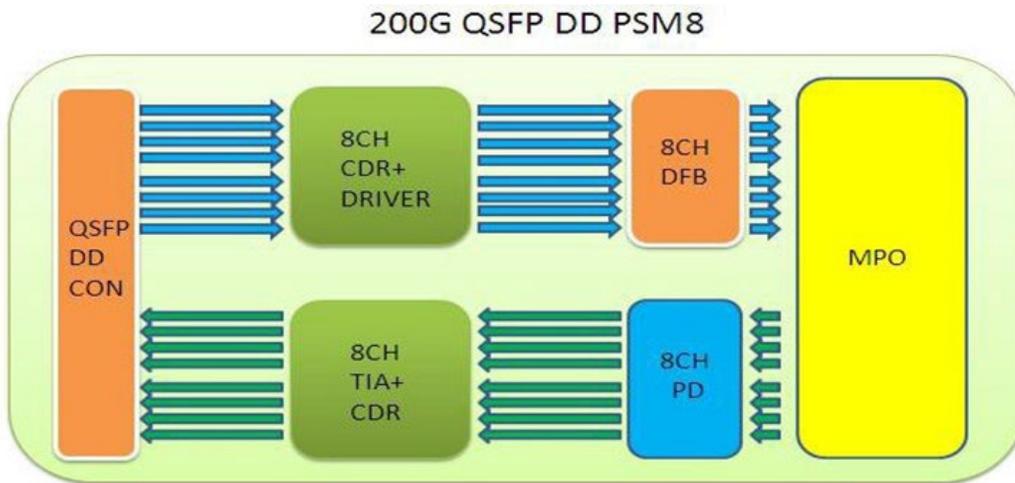
**Electrical Pin-Out Details**



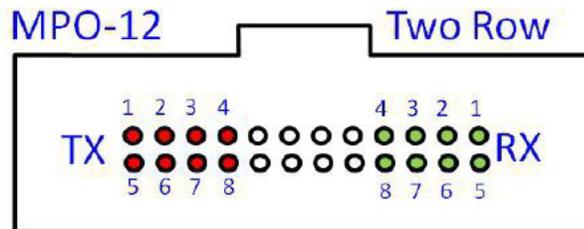
### Recommended Supply Filter



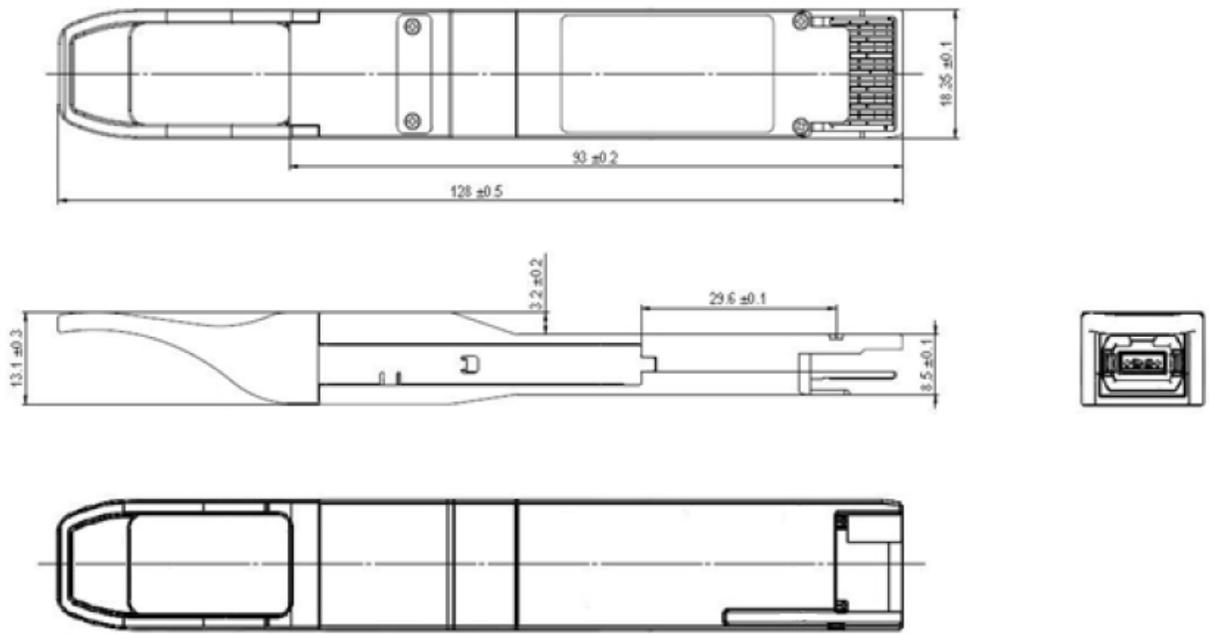
### Block Diagram



### Optical Interface Lanes and Assignments



# Mechanical Specifications



## About AddOn Networks

In 1999, AddOn Networks entered the market with a single product. Our founders fulfilled a severe shortage for compatible, cost-effective optical transceivers that compete at the same performance levels as leading OEM manufacturers. Adhering to the idea of redefining service and product quality not previously had in the fiber optic networking industry, AddOn invested resources in solution design, production, fulfillment, and global support.

Combining one of the most extensive and stringent testing processes in the industry, an exceptional free tech support center, and a consistent roll-out of innovative technologies, AddOn has continually set industry standards of quality and reliability throughout its history.

Reliability is the cornerstone of any optical fiber network and is engrained in AddOn's DNA. It has played a key role in nurturing the long-term relationships developed over the years with customers. AddOn remains committed to exceeding industry standards with certifications from ranging from NEBS Level 3 to ISO 9001:2005 with every new development while maintaining the signature reliability of its products.



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